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Analysis and Performance Investigation of a Cascaded Multilevel STATCOM for Power System Voltage Regulation

Nitus Voraphonpiput[*1], Teratam Bunyagul[+] and Somchai Chatratana[#]

Abstract- *This paper presents an analysis of a cascaded multilevel STATCOM based on space vector theory. Simple relationships between reactive current, capacitor current and delayed angle are derived from the steady state analysis. The switching pattern design and the optimization technique to achieve the output voltage waveform which conforms to the IEC standard for harmonics are described and the design results are verified by the harmonics analysis. A typical 230 kV power system with a 100 MVA cascaded 5-link, 11-level STATCOM is simulated on PSCAD/EMTDC digital simulator. Due to unequal duty cycles, the voltage drops across DC capacitors of the converters are unequal and a simple voltage equalization technique without additional control loop is proposed. The dynamic performances of the casc aded multilevel STATCOM, which was subjected to disturbances and change of commands, are illustrated. Simulation results indicate that the proposed system can provide fast reactive current response and fast equalization the DC capacitor voltages. The harmonics content of the output voltage waveform can be controlled within an acceptable level even it is only a 5-link, 11-level cascaded STATCOM.*

Keywords - STATCOM, FACTS, Cascaded Multilevel Converter, Voltage Regulation.

1. INTRODUCTION

In recent years, the voltage source based Flexible AC Transmission System (FACTS) controllers have been widely used in many utilities. FACTS controllers are employed as Static Synchronous Compensators (STATCOM) in the power system. The STATCOM acts as a synchronous voltage source which can supply or consume reactive current at the point of common coupling. In comparison with the traditional reactive compensator, the STATCOM offers better dynamic response and wider range of compensation with smaller installation area. The conventional STATCOM uses multi-pulse configuration to generate an output voltage with the waveform which is close to sinusoidal waveform. In general, a magnetic interface, which consists of zigzag transformers, is necessary for this configuration. The zigzag transformers are bulky, heavy, and uneconomic, due to the losses associated with the transformers.

In 1996, three multi-level circuits for power application were reported [1]. They are diode-clamp circuit, flying-capacitor circuit, and cascaded-converter circuit. These configurations do not require magnetic interface, therefore the construction cost and installation area can be reduced. However, the clamping diode and flying-capacitor circuits are difficult to realize at high voltage and high power [2], [3]. This is because these circuits require very large number of clamping diodes or flying capacitors connected in series to withstand the voltage. It does not only increase the component cost but also causes problem in packaging. Thus, the clamping diode and flying-capacitor circuits are not suitable for STATCOM circuit.

Another approach is to use cascaded multi-level converter circuit. The cascaded converter circuit consists of several H-bridge converters connected in series. A DC capacitor is connected to the output side of each converter to act as a voltage source. All H-bridge converters can be designed as similar modules of the same rating and packaging. The quality of the output voltage waveform can be improved by increasing the number of the cascaded converters. Multiple converters result in reduction of the rating of each converter. The cascaded converter circuit, which is also known as cascaded multi-level circuit or circuit with Chain-Link topology, is easy to realize [4], [5]. Therefore, it is believed that the cascaded multi-level circuit will become a standard STATCOM circuit. Nevertheless, the unbalanced DC voltage drops across capacitors and harmonics are still two major problems in this circuit [5], [6]. The unbalanced capacitor voltages normally occur due to the difference in parameters of the switching devices and the unequal switching duty. Several techniques such as control loop for balancing DC capacitor voltage, additional voltage balancing circuit and single pulse rotation technique are adopted to mitigate this problem [3], [7], [8].

In this paper, the principle of operation of a STATCOM and its steady state performance are analyzed in section 2. In section 3, a cascaded multilevel converter circuit and the generation of output voltage are described. The switching pattern design is explained in section 4. The optimization technique and IEC 61000-3-6 standard are used to determine the switching pattern, which produces the output voltage that meets the harmonics

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criteria. In section 5, the problem of unbalanced DC capacitor voltages is discussed and the fractional MVA inverters with a common AC bus are proposed to solve the problem. A digital simulation was performed on a power system with a 100 MVA cascaded 5-link, 11-level STATCOM and the simulation results are presented in section 6.

2. MATHEMATICAL MODELING

An equivalent circuit of a simple two-bus system is shown in Fig. 1, where R and L represent the equivalent circuit resistance and inductance of the electrical system between bus 1 and 2. The voltage at bus 2 is the output voltage of the STATCOM which is assumed to be quasi-sinusoidal. Three-phase instantaneous phase voltages at bus 1 and bus 2 are u_a, u_b, u_c and v_a, v_b, v_c, respectively. Instantaneous line currents are i_a, i_b and i_c.

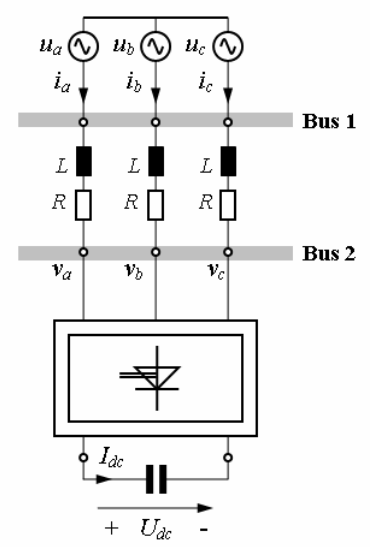

Fig. 1. An equivalent circuit of a simple two bus power system with a STATCOM circuit.

The space vector theory based on synchronously rotating reference frame (dq-axis) is applied to the voltage equations of the two bus power system. The space vector diagram in Fig. 2 shows the $\alpha\beta$-axis which represents the stationary reference frame and the dq-axis which represents the synchronously rotating reference frame. The synchronously rotating reference frame displaces from the stationary reference frame by an angle λ.

Two complex voltage vectors and a complex current vector can be expressed in the stationary rotating reference frame ($\alpha\beta$-axis) as

$$\underline{U} = \frac{2}{3}\left\{u_a + u_b\, e^{j\gamma} + u_c e^{j2\gamma}\right\} = U\, e^{j\lambda} \tag{1}$$

$$\underline{V} = \frac{2}{3}\left\{v_a + v_b\, e^{j\gamma} + v_c e^{j2\gamma}\right\} = V\, e^{j(\lambda-\delta)} \tag{2}$$

$$\underline{I} = \frac{2}{3}\left\{i_a + i_b\, e^{j\gamma} + i_c e^{j2\gamma}\right\} = I\, e^{j(\varphi+\lambda)} \tag{3}$$

Where

$$\gamma = \frac{2\pi}{3}$$

δ is the delayed angle of the voltage vector $\underline{V}$ with respect to the d axis

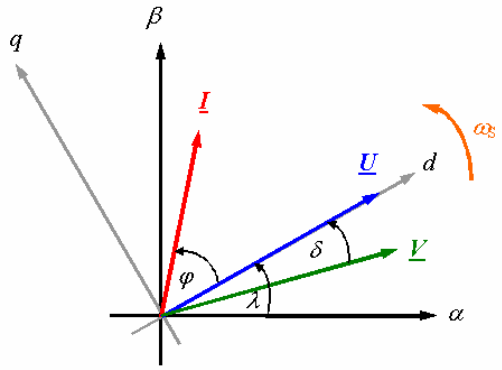

Fig. 2. Space vector diagram of voltages and current in synchronously rotating reference frame (dq) and stationary reference frame ($\alpha\beta$).

The d-axis of the space vector diagram in Fig. 2 is assigned to coincide with the space vector $\underline{U}$. The voltage equation with reference to the stationary reference frame ($\alpha\beta$-axis) can be written as

$$L\frac{d\underline{I}}{dt} + R\underline{I} = \underline{U} - \underline{V} \tag{4}$$

The complex vectors in the stationary reference frame are transformed onto the synchronously rotating reference frame by multiplying every term of (4) with a unit space vector $e^{-j\lambda}$.

$$L\, e^{-j\lambda}\frac{d\underline{I}}{dt} + R e^{-j\lambda}\underline{I} = \underline{U} e^{-j\lambda} - \underline{V} e^{-j\lambda} \tag{5}$$

$$\underline{U} e^{-j\lambda} = u_d + j u_q \tag{6}$$

$$\underline{V} e^{-j\lambda} = v_d + j v_q = v e^{-j\delta} = v\cos\delta - jv\sin\delta \tag{7}$$

$$\underline{I} e^{-j\lambda} = i_d + j i_q \tag{8}$$

Where

u_d is the voltage at bus 1 in direct axis
u_q is the voltage at bus 1 in quadrature axis
v_d is the voltage at bus 2 in direct axis
v_q is the voltage at bus 2 in quadrature axis
v *is the magnitude of voltage vector at bus 2*
i_d *is the current in direct axis*
i_q *is the current in quadrature axis*

Substituting (6), (7), (8) into (5) and rearranging the voltage equations for components on the d-axis and components for the q-axis as follows

$$L\frac{di_d}{dt} + Ri_d = u_d - v\cos\delta + L\omega_S\, i_q \tag{9}$$

$$L\frac{di_q}{dt} + Ri_q = u_q + v\sin\delta - L\omega_S\, i_d \tag{10}$$

where ω_S is the system frequency.

The peak value of the quasi-sinusoidal voltage waveform at bus 2 (v) is proportional to the voltage drop across the capacitor. Using Fourier's series expansion, the magnitude of the fundamental of component can be expressed as,

$$v = m U_{dc} \tag{11}$$

where

U_{dc} is the maximum DC voltage drops across the capacitors

m is a proportional factor which depends on the output voltage waveform of the converter.

If the converter losses are neglected, the power flow into the converter in the dq-axis equals to the instantaneous power of the DC capacitor which can be described as

$$P = U_{dc} I_{dc} = \frac{3}{2}\left(v_d i_d + v_q i_q\right) \tag{12}$$

where

I_{dc} is the capacitor current

Therefore, the DC current can be expressed as

$$I_{dc} = \frac{3}{2} m\left(i_d \cos\delta - i_q \sin\delta\right) = C\frac{dU_{dc}}{dt} \tag{13}$$

where

U_{dc} is the maximum DC voltage drop across the capacitor.

Equation (9), (10), and (13) form a state equation for the STATCOM,

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{1}{T_1} & \omega_S & -\frac{m}{L}\cos\delta \\ -\omega_S & -\frac{1}{T_1} & \frac{m}{L}\sin\delta \\ \frac{3}{2}\frac{m}{C}\cos\delta & -\frac{3}{2}\frac{m}{C}\sin\delta & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{14}$$

where $T_1 = \frac{L}{R}$

Steady state performance of the STATCOM can be expressed by setting all derivative terms in (14) to zero, which results in

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega_S & -\frac{m}{L}\cos\delta \\ -\omega_S & -\frac{R}{L} & \frac{m}{L}\sin\delta \\ \frac{3}{2}\frac{m}{C}\cos\delta & -\frac{3}{2}\frac{m}{C}\sin\delta & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{15}$$

Since u_d is located on d-axis, at steady state, the voltage on the direct axis (u_d) equals to the voltage at bus 1 (U) and the voltage on the quadrature axis (u_q) becomes zero. Consequently, the equation (15) can be rewritten as

$$\begin{bmatrix} -R & \omega_S L & -m\cos\delta \\ -\omega_S L & -R & m\sin\delta \\ 3m\cos\delta & -3m\sin\delta & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} = -\begin{bmatrix} U \\ 0 \\ 0 \end{bmatrix} \tag{16}$$

Solving for i_d, i_q and U_{dc}, the solutions are

$$i_d = \frac{\sin^2\delta}{R} U \tag{17}$$

$$i_q = -\frac{\sin\delta\cos\delta}{R} U \tag{18}$$

$$U_{dc} = \frac{\left(R\cos\delta + \omega_S L\sin\delta\right)}{Rm} U \tag{19}$$

In (17), (18) and (19), i_d, i_q, and U_{dc} are the functions of the delayed angle (δ) and voltage source at bus 1 (U). Since the voltage source at bus 1, the resistor (R) and the inductor (L) are constant, the i_d, i_q, and U_{dc} can be controlled by the delayed angle (δ).

Equations (17) to (19) do not include the capacitance (C) of the DC capacitor. Therefore, the capacitance of DC capacitor has no effect on i_d, i_q, and U_{dc} in the steady state operation. However, the DC capacitor acts as DC voltage source which can supply or absorb reactive power between the power system and the STATCOM. The capacitance value can be selected to meet the economic and harmonic criteria. It can also be determined by the expression

$$C = \frac{2\tau S}{U_{dc}^2} \tag{20}$$

where

τ is the time, which is in the range of 15-30 ms [9].

S is the VA rating of the STATCOM.

The steady state performance are shown in Fig. 3, in terms of active current (i_d), reactive current (i_q) and capacitor voltage (U_{dc}) as a function of the delayed angle (δ). They were calculated from (17), (18) and (19) with typical parameters: of $R = 0.035$ pu, $\omega_S L = 0.15$ pu and $m = 1.028$.

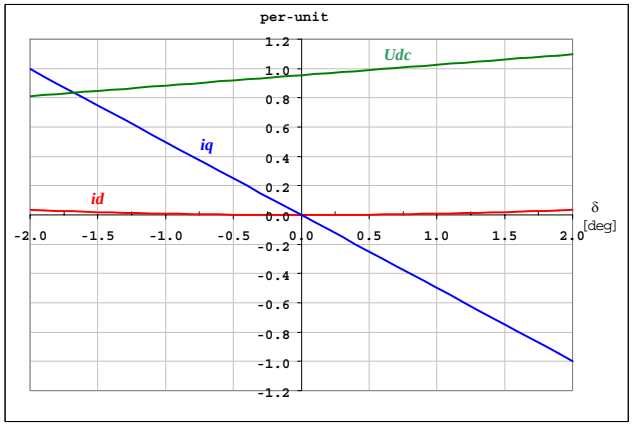

Fig. 3. Steady state characteristic of the STATCOM.

It can be seen from Fig. 3 that the reactive current (i_q) varies linearly with the delayed angle (δ). The STATCOM supplies reactive current to the power system when it is operating with positive delayed angles and absorbs reactive current from the power system when it is operating with negative delayed angles. Note that the range of the delayed angles is very small and the rated reactive current reaches 1.0 per-unit at the delayed angle of ±2 degrees. The active current (i_d), which indicates power losses in the STATCOM system, is small and varies with the delayed angle (δ) within a small range. The main losses occur in the resistive components of the electrical system.

The DC capacitor voltage also increases linearly from the negative delayed angle to the positive delayed angle (δ). The DC voltage is high when the STATCOM generates the reactive current and it is low when the STATCOM absorbs the reactive current.

3. CASCADED MULTILEVEL CIRCUIT

The cascaded multilevel STATCOM circuit shown in Fig.4 comprises five single phase H-bridge voltage source converters, connected in series in each phase. The three phase configuration can be made in the form of Wye or Delta connection. Each single phase bridge converter has four arms. Each arm consists of a GTO and a diode connected in anti-parallel to form a two-way switch. Each single phase converter has its own capacitor, acting as a voltage source. Individual capacitor of the same

capacitance is selected to meet economic and harmonics criteria. Theoretically, it can be assumed that the voltage drop across each capacitor (U_{dc}) is equal. At any interval of time, the output voltage of each phase is the summation of the output voltage of individual converter, which can be positive, negative or zero. A STATCOM with N converters per phase can synthesize *2N+1* voltage levels. The maximum output voltage of the STATCOM is *N* times of the capacitor voltage (U_{dc}).

In the high voltage and high power application, the two-way switch is switched on and off once per cycle to avoid high switching losses. Individual converter produces a square wave voltage with the magnitude of positive U_{dc}, zero or negative U_{dc}. If the switching angle of the converter 1 is θ_1, the positive U_{dc} pulse starts at the angle θ_1 and ends at the angle π-θ_1. The positive pulse is followed by zero voltage between π-θ_1 and π+θ_1. The negative U_{dc} pulse starts at π+θ_1 and ends at 2π-θ_1. Other converters operate in the same fashion as the converter 1, but with different pulse widths. The number of the converters (*N*) must be high enough to achieve good quality of sinusoidal voltage waveform. Fifteen converters connected in series can be found in practice [7]. The output voltage waveforms of the Cascaded *N*-level STATCOM are illustrated in Fig. 5.

The cascaded multilevel STATCOM can be directly connected to the power system via a conventional power transformer. Small reactors (X_s) in Fig.4, are air core reactors. These reactors limit voltage and current stresses on the GTOs and diodes in the event of faults on the converter side [7]. Moreover, the small reactor can perform as harmonic filter. The typical value of the small reactor is 0.2 p.u. based on voltage and current rating of the inverter [8]. The small reactor can also be considered as the leakage reactance of the power transformer in some designs.

4. SWITCHING PATTERN DESIGN

It can be seen from Fig. 5 (a) that the output voltage waveform of the cascaded *N*-level STATCOM is quasi-sinusoidal and depends on the switching angles of the converters. These switching angles (θ_1 to θ_N) can be independently selected to achieve good quality of the output voltage waveform. Many techniques for harmonics reduction or harmonics elimination are well known, such as: elimination of the low order odd harmonics [3], [6], minimization of harmonics which its order is less than 25^{th} [2], maximization of fundamental component and elimination of low order harmonics [7], [10].

In this paper, a cascaded 5-link, 11-level STATCOM is assumed to connect to a medium voltage bus (1 to 35 kV). The investigation of switching pattern design starts with two common methods, namely the Elimination of 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} order harmonics (Design A) and the minimization of Total Harmonic Distortion (Design B). In order to conform to utilities' requirement, it is proposed that another constraint on harmonics levels (IEC 6100-3-6 standard) should be included. In Design C, limits according to IEC standard are incorporated into the minimization of the 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} order harmonics and in Design D the limits according to IEC standard are incorporated into the minimization of total harmonic distortion. The switching pattern design methods are described in Table 1. The limits of the magnitude of harmonic voltages and THD according to IEC 61000-3-6 are given in Table 2.

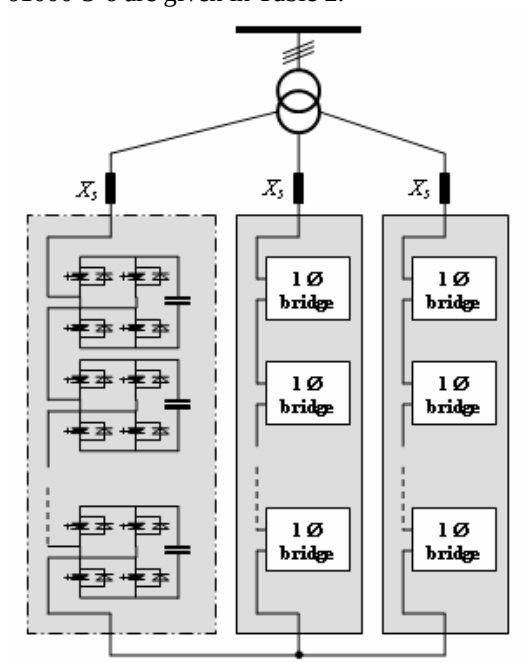

Fig. 4. Wye connected cascaded multilevel STATCOM.

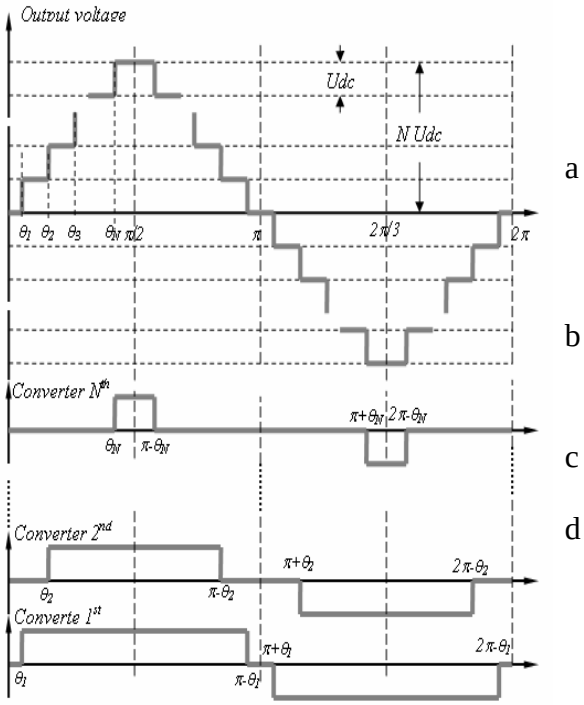

Fig. 5 Output voltage waveform of a Cascaded N-level STATCOM (a) and the voltage waveform of individual inverter (b,c, and d).

Table 1. Switching Pattern Design Methods

Design A	Elimination of the 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} harmonic orders
Design B	Minimization of Total Harmonic Distortion (THD)
Design C	Minimization of the 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th} harmonic orders with IEC 61000-3-6 constraints
Design D	Minimization of Total Harmonic Distortion (THD) with IEC 61000-3-6 constraints

Table 2. Planning Levels for Harmonic Voltages (in Percentage of Fundamental) for Medium Voltage Level (1-35 kV) according to IEC 61000-3-6

Harmonic order	Harmonic voltage (%)
5	5
7	4
11	3
13	2.5
17	1.6
19	1.2
23	1.2
25	1.2
THD	6.5

Using Fourier's series method, the amplitude of the odd order harmonic of the output voltage with *2N+1* level, can be described in (1).

$$u_n = \frac{4U_{dc}}{n\pi}\sum_{k=1}^{N}\cos(n\theta_k) \tag{1}$$

where

u_n is the amplitude of voltage harmonic of n^{th} order
U_{dc} is the DC voltage drop across the capacitor
N is the number of the converters in each phase
n is the odd order harmonic
θ_k is the switching angle of the single phase bridge converter k^{th}

In Design A, the harmonics elimination method is employed. The numbers of eliminated harmonics are equal to the number of the converters (*N*), thus the selected order harmonics to be eliminated are 5th, 7th, 11th, 13th and 17th order because these low order harmonics can cause resonance in the power system. The selected harmonic voltages are set to zeros. Rearranging the equation results in

$$\begin{aligned}
&\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+\cos(5\theta_5)=0\\
&\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)+\cos(7\theta_5)=0\\
&\cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)+\cos(11\theta_5)=0\\
&\cos(13\theta_1)+\cos(13\theta_2)+\cos(13\theta_3)+\cos(13\theta_4)+\cos(13\theta_5)=0\\
&\cos(17\theta_1)+\cos(17\theta_2)+\cos(17\theta_3)+\cos(17\theta_4)+\cos(17\theta_5)=0
\end{aligned} \tag{21}$$

The equation (21) is a set of nonlinear transcendental equations with possible solutions and impossible solutions. Possible solutions will be in the range of θ_n from 0 to π/2 radians because the switching angles (θ_1, θ_2, θ_3, θ_4 and θ_5) cannot be greater than π/2 radians or 90 degrees and it cannot be smaller than 0 degrees. The Newton's method is generally used to solve nonlinear transcendental equations but in this paper the optimization technique is applied. The harmonics elimination can be solved by using the objective function in (22).

$$Minimize J = \sum_{h=5,7,11,13,17}\{u_h(\theta_h)\}^2 \tag{22}$$
$$Subject\ to \quad \frac{\pi}{2} \geq \theta_h \geq 0$$

In Design B, the total harmonic distortion (THD) of the output voltage waveform is selected as an objective function. The optimization technique is applied to minimize the THD. The objective function can be written as

$$Minimize\ J = \frac{\sqrt{\sum_{h>1}^{25}\{u_h(\theta_h)\}^2}}{u_1},\ h = 3,5,7,....,25 \tag{23}$$
$$Subject\ to \quad \frac{\pi}{2} \geq \theta_h \geq 0$$

The minimization of 5th, 7th, 11th, 13th and 17th order harmonics is the main technique of the Design C and the IEC 61000-3-6 standard is used as inequality constraints. The objective function and its constraints can be written as

$$Minimize J = \sum_{h=5,7,11,13,17}\{u_h(\theta_h)\}^2$$
$$Subject\ to$$
$$\begin{aligned}
&\frac{\pi}{2} \geq \theta_h \geq 0\\
&u_n(\theta_n) <= v_n \quad n = 5,7,11,13,15,17,19,23,25\\
&THD <= THD_{\max}
\end{aligned} \tag{24}$$

where v_n is the acceptable amplitude of the n^{th} harmonic.

The minimization of output voltage waveform THD and IEC 61000-3-6 standard are the design criteria in Design D. The objective function and its inequality constraints can be written as

$$Minimize\ J = \frac{\sqrt{\sum_{h>1}^{25}\{u_h(\theta_h)\}^2}}{u_1}$$
$$Subject\ to \quad \frac{\pi}{2} \geq \theta_h \geq 0$$
$$u_n(\theta_n) <= v_n \quad n = 5,7,11,13,15,17,19,23,25 \tag{25}$$

The elimination and minimization of all designs were solved by Nonlinear Programming with Quasi-Newton algorithm. Optimal solutions obtained from Design A to Design D are presented in Table 3 and the harmonics content in the output voltage waveforms in percentage of the fundamental voltage are present in Table 4.

From Table 4, Fig. 6, and Fig. 7, it can be seen that Design A can completely eliminate the 5th, 7th, 11th, 13th, and 17th order harmonics but the 19th and the 23rd order, and the total harmonic distortion are higher than the limits given by the IEC standard. Design B gives the lowest total harmonic distortion within the limit as planned but the 25th order harmonic exceeds the limit. In order to improve the waveform with these two designs, the number of converters must be increased.

Table 3. Switching Angles from Four Design Methods

	θ_1	θ_2	θ_3	θ_4	θ_5
Design A	6.57°	14.76°	23.61°	37.04°	58.06°
Design B	6.56°	16.94°	28.17°	43.05°	60.32°
Design C	7.28°	18.03°	28.48°	44.18°	60.45°
Design D	7.19°	17.35°	28.50°	43.05°	61.33°

Table 4. Harmonics content of the Output Voltage Waveform in Percentage of Fundamental Component

Order	Design A	Design B	Design C	Design D
5	0.00	0.67	1.05	0.72
7	0.00	0.87	0.64	0.17
11	0.00	0.24	0.24	0.45
13	0.00	0.37	0.19	0.95
17	0.00	1.47	1.38	1.60
19	1.90	0.66	1.20	1.20
23	1.92	0.98	1.20	1.20
25	0.51	1.79	1.20	1.20
THD	7.71	5.89	6.12	5.97

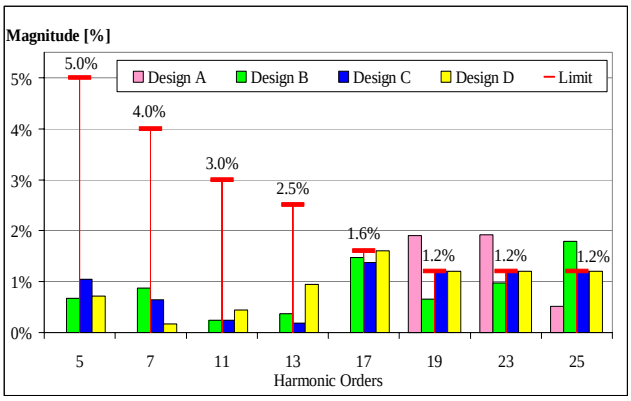

Fig. 6. Odd harmonic content of the output waveform from Design A to D and harmonic voltage limits from IEC 61000-3-6.

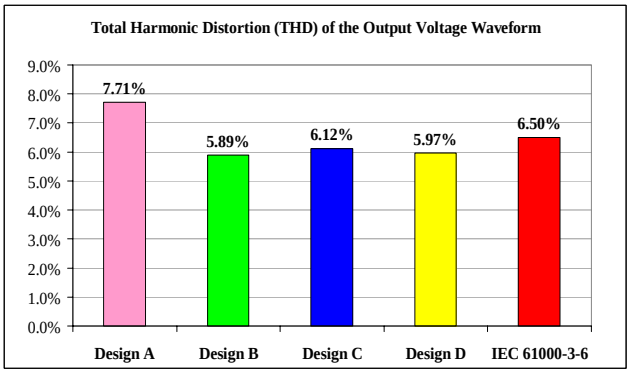

Fig. 7. Comparison of THD from Design A to D and THD limit from IEC 61000-3-6.

When the constraints of harmonic limits according to IEC 61000-3-6 are incorporated into the minimization process in Design C, THD of 6.12 % can be achieved. This is lower than the limit THD which is 6.5%. Although the 5th, 7th, 11th, 13th and 17th order harmonics are not zero, it can be seen from Fig. 6 that they together with the 19th, 23rd and 25th order harmonic are lower than the harmonic limits.

Minimization of THD with harmonics limit constraints is employed in Design D. This design gives the THD of 5.97% and harmonic content of all harmonics is lower than the limit. It can be observed that the percentages of 19th, 23rd and 25th order harmonics are the same for Design D and Design C (1.2%). Design D gives lower 5thand 7th order harmonics when compares to Design C. However, the 11th, 13th and 17th order harmonics are higher that the Design C. Low order harmonics can cause electrical resonance in the power system. For this reason, design D is the most favorable method for this converter circuit.

5. EQUALIZATION OF DC CAPACITOR VOLTAGE

The differences in parameters from one switching device to another switching device and unequal switching duty of each converter result in unequal charging and discharging of each dc capacitor. This unequal charging, in turn, leads to unequal voltage drop across each capacitor. Divergence of the capacitor voltages in the same phase is reported in [11], [12].

Fig. 8 shows a typical 230 kV 50 Hz radial transmission system with the short circuit MVA of 3,000 MVA. A 100 MVA cascaded multilevel STATCOM is connected to the receiving end bus (bus *U*) which also connects to a load of 150 MVA with 0.87 lagging power factor. The cascaded 11 level STATCOM is connected to the system via a 230 kV/15 kV 100 MVA transformer with 10% impedance. The transformer is connected in Wye-Delta (*YD11*).

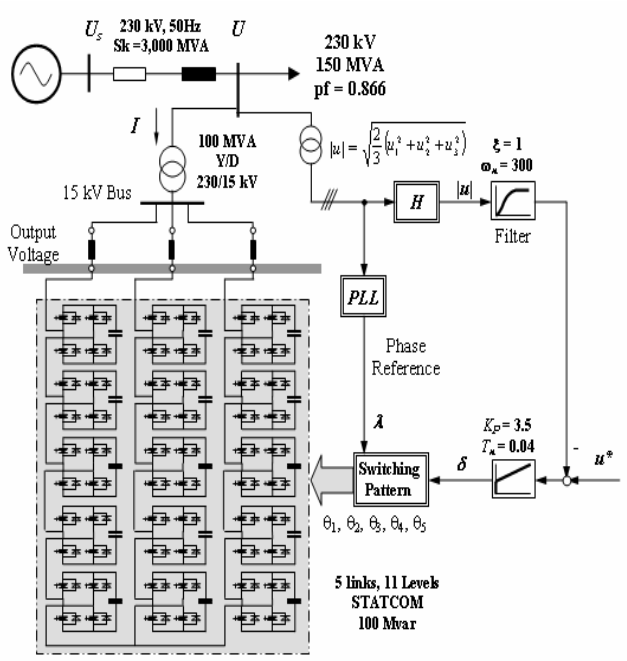

Fig. 8. The diagram of 230 kV system with short circuit rating of 3000 MVA with voltage regulation by STATCOM.

Three-phase bus voltages are measured and used to calculate the voltage magnitude at the block *H*. The magnitude calculation block provides a voltage magnitude signal (|*u*|), which is filtered and then compared with the reference voltage signal (*u**). The proportional plus integral controller (PI-Controller) is employed to achieve fast voltage dynamic response. The PI controller provides necessary delayed angle (δ) for the switching pattern generation block. The three phase bus voltages are fed into Phase Locked Loop (*PLL*) block to calculate the reference phase angle (λ), which is also used in conjunction with the angle command (δ) for switching pattern generation.

The power system with 100 MVA cascaded 11-level STATCOM, was simulated on PSCAD/EMTDC. Capacitor voltages of the converters in phase A of the STATCOM during start up are presented in Fig. 9. In this

case, each converter produced its output voltage according to the switching pattern generated by design D. Transients can be seen during 0.0–0.1 second and steady state voltages across capacitors (U_{dc1}, U_{dc2}, U_{dc3}, U_{dc4} *and* U_{dc5}) are not equal. The base voltage for this calculation is 12.25 kV.

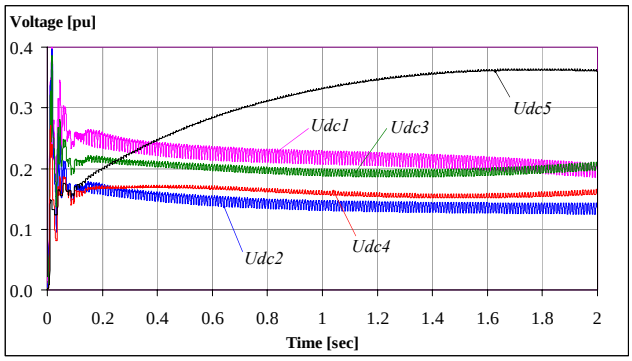

Fig. 9. DC capacitor voltage of each converter during startup.

In Fig. 10, the STATCOM converters were initially switched with full duty cycle (0° to 180° and 180° to 360°) to ensure that all capacitor voltages were equal. The converters were then switched to the design D switching pattern at 0.3 seconds. It can be seen that all capacitor voltages are equal at first (up to 0.3 second). After switching to normal operation at 0.3 second, each capacitor voltage assumes its own dc voltage according to its switching duty. These simulation results indicate that the unbalanced capacitor voltage always occurs no matter what voltage level it is started with.

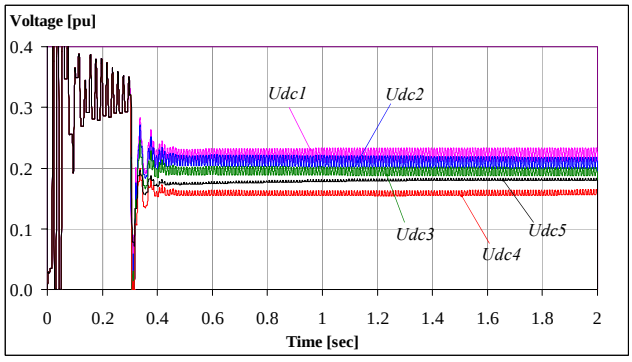

Fig. 10. DC capacitor voltage of each converter when startup from equal DC voltage.

Many strategies have been reported in literature to overcome this problem [3], [7], [8] and [12]. Almost all strategies are related to the manipulation of the switching pattern such as, unsymmetrical switching pattern, cycling duty cycles, etc. They normally require an additional control loop to equalize the capacitor voltage. Additional control loop normally slows down the dynamic response of the voltage control loop and it is difficult to avoid the interference between the additional control loop and other control loops.

Instead of an additional control loop, auxiliary inverter circuits and a common ac bus are proposed here to balance the capacitor voltages as shown for one phase of the converter in Fig. 11. The overvoltage caused by overcharging of one capacitor is transferred to a common ac bus via a transformer. This excess voltage can be used to charge the undercharged capacitor. The capacitor voltages will be naturally balanced by the common ac bus. Small energy transfer occurs during the balancing of capacitor voltage, therefore the rating of each auxiliary inverter is only a fraction of the rating of the STATCOM.

In this paper, five fractional MVA inverters with the rating of 300 kVA (or 4.5% of a H-bridge converter) are used in each phase. It can operate at high switching frequency up to kilohertz [12]. Thus, the transformer can be small. In this simulation, the fractional MVA inverters were assigned to operate at 500 Hz to reduce simulation time.

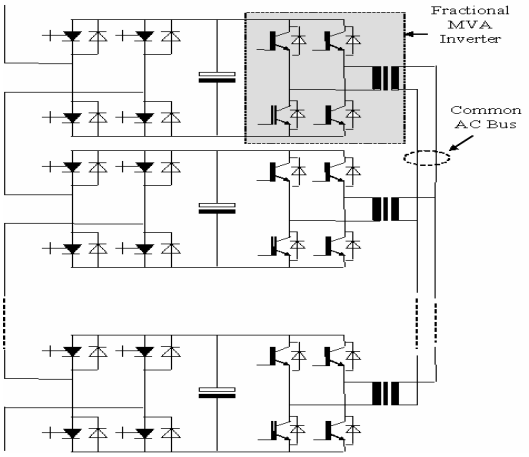

Fig. 11. Auxiliary inverters and a common AC Bus.

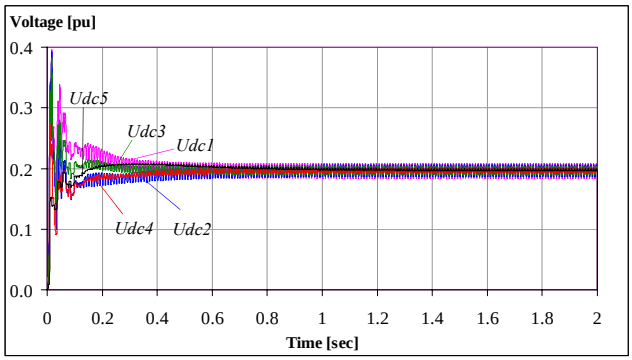

Fig. 12. DC capacitor voltage of each converter during startup.

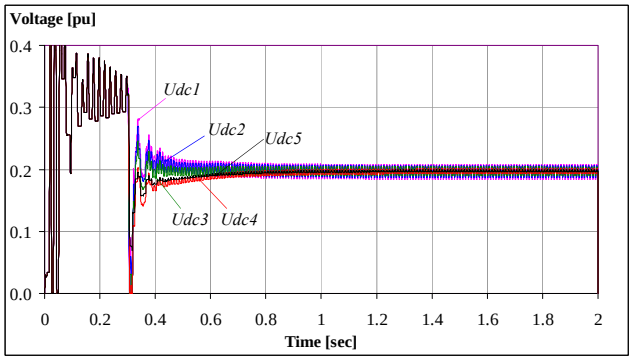

Fig. 13. DC capacitor voltage of each converter when startup from equal DC voltage.

The STATCOM with auxiliary inverters was simulated with the same conditions as in Fig. 9 and Fig.10 and the results are shown in Fig. 12 and Fig. 13 respectively. In Fig. 12, it can be seen that after transient, the capacitors were equalized within 0.8 second. In Fig. 13 the capacitor voltages are equal during 0.0 to 0.3 second due to equal switching duty. After switching to

unequal switching duty at 0.3, transient occurred but all capacitor voltages were settled and equalized within 0.8 second.

6. SIMULATION RESULTS

The power system with a STATCOM (including auxiliary inverters) was simulated for three events to test the dynamic response of STATCOM. The voltage at the receiving end was previously controlled to 1.0 p.u. (Pre-event) by the STATCOM. The first event (Event 1) was initiated at 1.0 second, when a 50 MVA load was rejected from the bus. The second event (Event 2) was initiated at 1.4 seconds, in which the reference voltage (u^*) was reduced from 1 p.u. to 0.97 p.u. Finally, the third event (Event 3) occurred at 1.8 seconds, when the reference voltage was increased from 0.97 p.u. to 1.01 p.u.

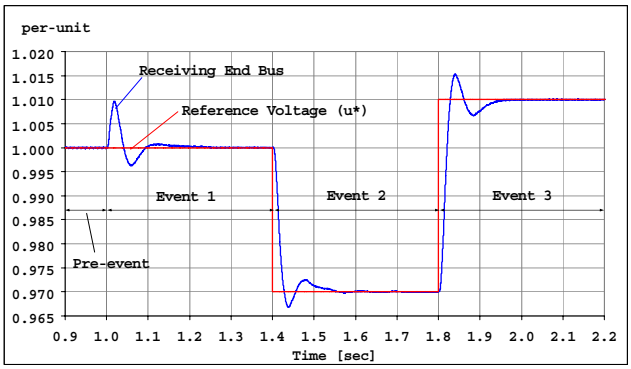

Fig. 14. Receiving end voltage and Reference Voltage

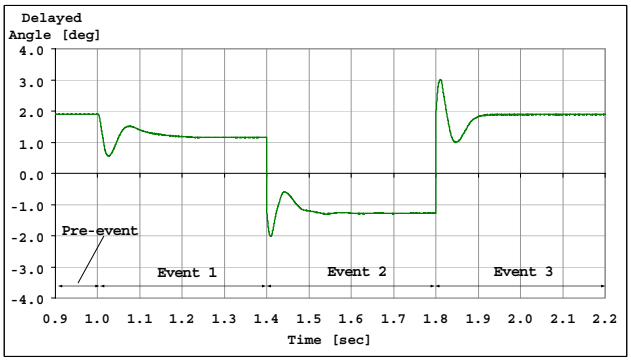

Fig. 15. Response of the Delayed angle (δ).

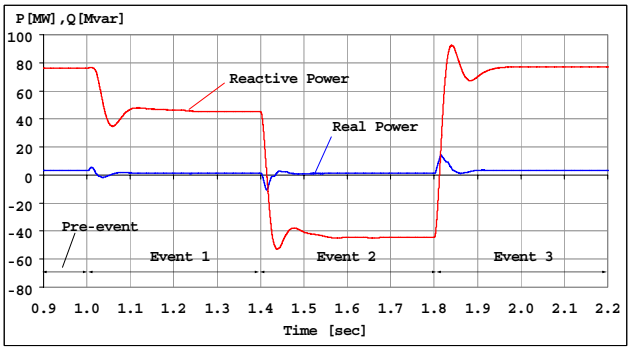

Fig. 16. Real and reactive power of the STATCOM.

When the 50 MVA load was tripped from the system at 1.0 second. It can be seen from Fig. 14 that the receiving end voltage increased to 1.01 p.u. and then recovered to 1.0 p.u. within 0.15 second, due to the action of the PI-controller. To respond to load rejection the PI controller reduced the delayed angle (δ) from +1.89 degrees to +1.16 degrees as shown in Fig. 15. It can also be seen in Fig. 16 that the reactive power from STATCOM was reduced from +76 Mvar to +45 Mvar due to the reduction of the delayed angel (δ). The reduction of reactive current from -0.75 per unit to -0.46 per unit is shown in Fig. 17.

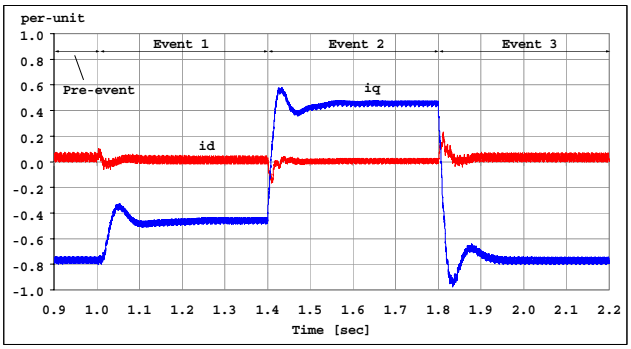

Fig. 17. Active current (id) and reactive current (iq) of the STATCOM.

In the second event (t = 1.4 seconds), the receiving end voltage reduced to 0.97 per-unit following a step change of the reference voltage (u^*). The receiving end voltage took approximately 0.15 seconds to settle. It can be seen in Fig. 15 that the delayed angle (δ) was switched from +1.16 degrees to -1.27 degrees. The STATCOM also changed from generating +45 Mvar reactive power to absorbing -45 Mvar reactive power in Fig. 16. The reactive current jumped from -0.46 per unit to +0.46 per unit within 0.15 second (from 1.4to 1.55 seconds) in Fig. 17.

The third event, which is a step change of reference voltage from 0.97 per unit to 1.01 per unit, occurred at 1.8 seconds. The receiving end voltage in Fig. 14 increased and settled at 1.01 per unit within 0.15 seconds. It can be seen in Fig. 15 that the delayed angle (δ) moved from -1.27 degrees to +1.89 degrees and the STATCOM changed from absorbing reactive power (-45 Mvar) to generating reactive power (+77 Mvar), which can be seen in Fig. 16 at t = 1.8 seconds. The reactive current in Fig.17 also moved from +0.46 per-unit to -0.77 per-unit and settled within 0.15 seconds (from 1.8 to 1.95 seconds).

Note that the real power in all events is positive. This indicates that the STATCOM always consumes real power no matter how much it absorbs or generates reactive power. This real power is required to maintain DC capacitor voltage and supplies converter losses.

Dynamic performances of the STATCOM were analyzed by means of voltage and current waveforms. The voltage and current waveforms of the first event (Event 1) are shown in Fig. 18. The current waveform leads the output voltage by almost 90 degrees. The STATCOM was generating reactive power at this moment. When the 50 MVA load was tripped at t = 1.0 seconds the output voltage reduced its amplitude to compensate the loss of load. It resulted in reduction of the current amplitude, which is shown in Fig. 18. Both waveforms settle within 1 cycle after the load tripping.

The voltage and current waveforms for the second event (Event 2) are shown in Fig.19. With a step change in the voltage reference, the current waveform changes from almost 90 degrees leading to almost 90 degrees lagging within 1 cycle. It shows that the STATCOM

changes very fast from generating reactive power to absorbing reactive power. It can also be observed that the amplitude of the output voltage waveform reduces after t = 1.4 seconds.

Figure 20 presents the voltage and current waveform during the third event (Event 3) when the voltage reference (u*) changed from 0.97 per-unit to 1.01 per-unit. The current waveform changes from almost 90 degrees lagging to almost 90 degrees leading within 1 cycle. Moreover, its amplitude also increases. It shows that the STATCOM can generate high level of reactive power, which conforms to the reactive power response in Fig. 15.

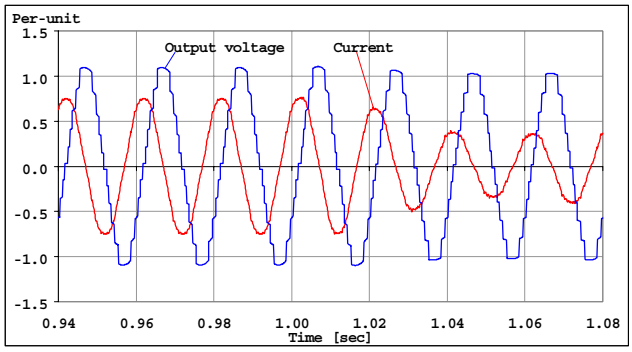

Fig. 18. Output voltage and current waveform of the STATCOM during Event 1.

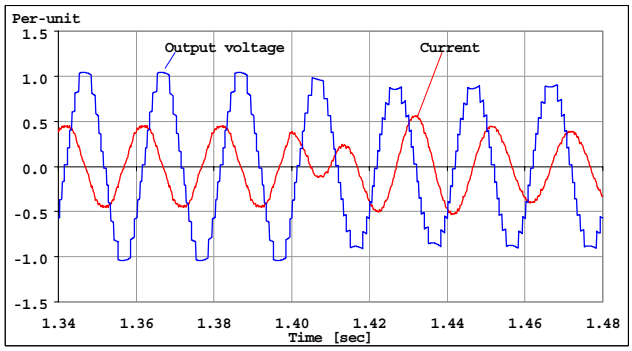

Fig. 19. Output voltage and current waveform of the STATCOM during Event 2.

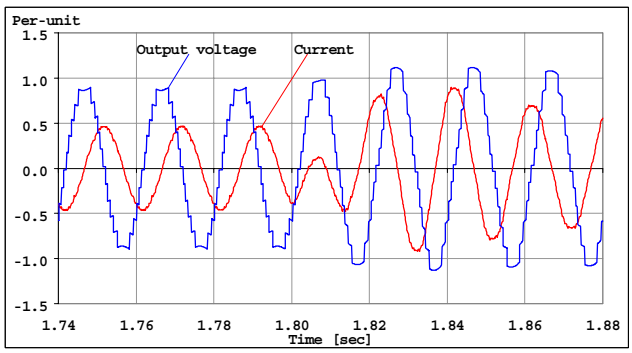

Fig. 20 Output voltage and current waveform of the STATCOM during Event 3.

Steady state performance of the STATCOM can be evaluated by its output voltage waveform. The output voltage waveform of H-bridge converters in phase A (VSC1 to VSC5) when absorbing reactive power (t = 1.76-1.8 seconds) are shown in Fig. 21. Each H-bridge converter operates at different switching angles and different duty cycles. The output voltage waveform of the STATCOM is the summation of output voltage of each converter connected in series. The output voltage waveform of the STATCOM and its current waveform are also shown in Fig.21.

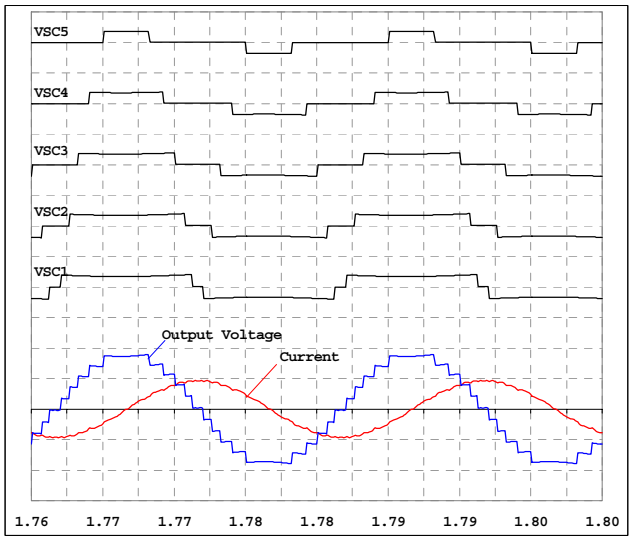

Fig. 21. The output voltage waveform of each H-bridge converter during absorbing reactive power.

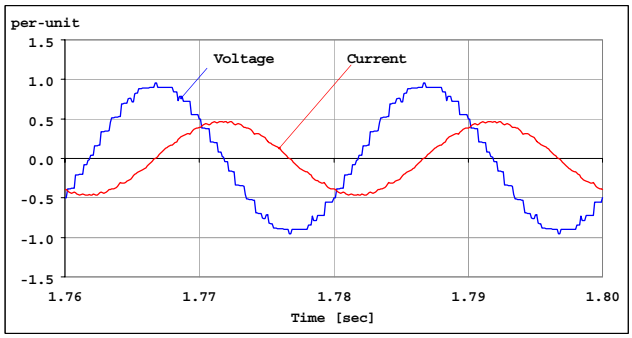

Fig. 22. The voltage and current waveforms of the secondary winding (15 kV bus) during absorbing reactive power.

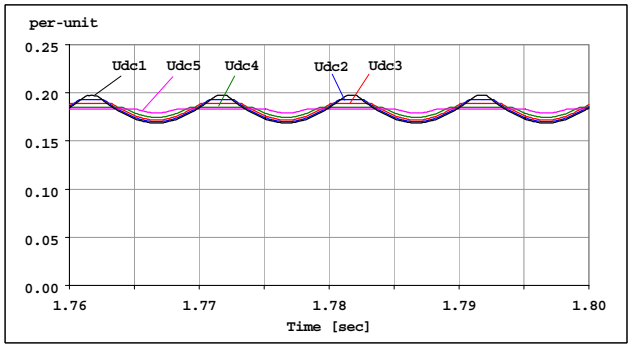

Fig. 23 Capacitor voltages during absorbing reactive power.

The STATCOM is connected to the secondary side of the transformer through a small three phase reactor (Fig. 8). The small reactor can reduce harmonics content in the output voltage waveform of the STATCOM. The waveforms of the transformer voltage and current at the secondary winding of phase A are presented in Fig. 22. Note that the voltage waveform is nearly sinusoidal.

Figure 23 shows voltage ripples in the DC capacitor voltages. The highest ripple occurs at the capacitor of the converter 1 (U_{dc1}) due to the longest switching pulses. It can be seen that duty cycle of the converter affects the DC capacitor voltage. Although the capacitor voltages have different ripples but the average dc voltages are

same.

The effect of voltage ripples in the capacitor voltage on harmonics content of the output voltage of STATCOM is investigated by the comparison of the output voltages obtained from the constant DC capacitor voltage and from the capacitor voltage with ripples. The spectrum of the harmonics content of the output voltage, from four cases of operation according to the delayed angles (δ = -2, -1, +1 and +2 degrees) with the switching pattern from design D and constant capacitor voltage, are shown in Fig. 24. It is very clear that harmonic content of the STATCOM output voltage waveform is very close to the design values. Harmonics content of the voltage waveform at the 15 kV Bus will be lower than the value given in Fig. 24 because the small reactors and the transformer act as low pass filters.

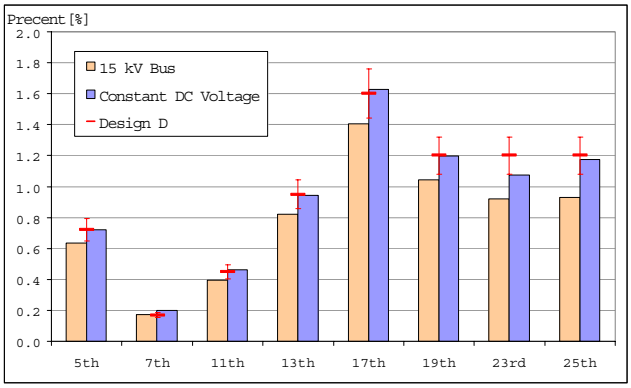

Fig. 24. Spectrum of 5th 7th 11th 13th 17th 19th 23rd 25th harmonics content of the output voltage waveform with constant dc voltage.

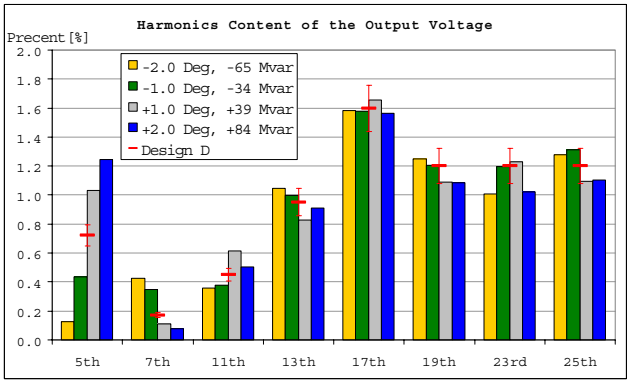

Fig. 25. Spectrum of 5th 7th 11th 13th 17th 19th 23rd 25th harmonics content of the output voltage waveform with ripples in the capacitor voltage.

Fig. 25 shows the spectrum of the harmonics content of the output voltage for the same operating conditions as in Fig. 24 but with ripples in the capacitor voltage. It can be seen that the 5th and 7th order harmonics are significantly higher than the design values in some cases. The STATCOM produces more 5th order harmonic when it generates reactive power and produces less 5th order harmonic when it absorbs reactive power. On the contrary, the STATCOM produces less 7th order harmonic when it generates reactive power and produces more 7th order harmonic when absorbs reactive power. Even though the 5th and 7th order harmonics are higher than the design values, all harmonics content is less than the harmonic limits given by IEC 61000-3-6.

Finally, the steady state operating points representing the DC capacitor voltage (U_{dc}), reactive current (i_q) and active current (i_d) versus the delayed angle (δ) are plotted for three events in Fig. 26.

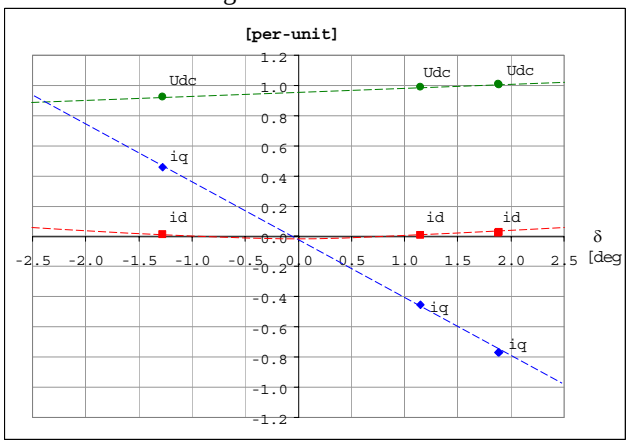

Fig. 26. Steady state performance of the STATCOM.

The dotted lines joining the same parameters from three events confirm the steady state analysis shown in Fig. 3. Moreover, it can be observed that the active current (i_d) is very small and it increases as a quadratic function of the delayed angle (δ).

7. CONCLUSION

The mathematical model of the cascaded multi-level STATCOM based on space vector theory was presented. Steady state analysis showed that reactive current and capacitor voltage varied linearly with the delayed angle. Moreover, the capacitance of the dc capacitor of the converter had no effect on the steady state performance. Effective control of reactive power can be achieved independently from the bus voltage by the control of delayed angles.

The switching pattern of each converter for the desired output voltage of the wye connected cascaded 11 level STATCOM was described in detail. Investigation on the optimum design of switching angles to obtain output voltage which conforms to the IEC 61000-3-6 was illustrated with four design cases. It was concluded that minimization of THD of the output voltage with harmonics content according to IEC standard gave most favorable solution. The proposed method could produce good quality output voltage without increasing the number of cascaded converters.

Simulation of a power system with 100 MVA cascaded 11-level STATCOM on PSCAD/EMTDC confirmed the unbalanced voltages of the dc capacitors. The unbalanced voltage produced distorted output voltage waveform and resulted in non-uniform ac voltage. An approach to solve this unbalanced capacitor problem by adding an auxiliary inverter to each converter and a common ac bus was proposed. Simulation results confirm that capacitor voltage could be equalized in a very short time and equal capacitor voltage could be maintained without additional control loop. Dynamic performances of the reactive power control were presented for three events of disturbances and command changes by the digital simulation. Detail analysis of current and voltage waveforms for each operating condition illustrated the action of the STATCOM controller. Effective and fast responses were achieved with the proposed circuit configuration, switching pattern design and control

scheme. Effects of ripple voltages on harmonics content of the output voltage were discussed and confirmed with the FFT spectrum analysis. Results from the responses of three events could also confirm the predicted steady state behavior obtained from space vector theory.

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