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Stability Analysis for the Grid-Connected Three-Phase Asymmetrical Cascaded Multilevel Inverter with Switched Capacitor Technique

Mohit Jain*, [1] A.N. Tiwari*, and A.K. Pandey*

Abstract – *Multilevel inverters (MLIs) have become increasingly popular for grid integration. This study introduces an innovative twenty-five-level switched-capacitor multilevel inverter (SCMLI) configuration specifically developed for applications in grid integration. The asymmetrical SCMLI generates a 25-level output voltage utilizing twelve power semiconductor switches, two diodes, two capacitors, and two asymmetric DC voltage sources with a quinary ratio. Unlike current designs, this topology features self-balancing capacitors without the need for additional circuitry, making it well suited for grid-connected applications that require higher voltage levels with fewer devices and a reduced total standing voltage (TSV). The inverter uses a level-shifted in-phase disposition (LS-IPD) multicarrier modulation technique to generate switching signals during the grid-connected operations. A comparative study with recent topologies highlighted the benefits of the proposed structure. Various operational modes are analyzed through simulations in MATLAB/Simulink.*

Keywords – LS-IPD, self-balancing, SCMLI, TSV, voltage gain.

1. INTRODUCTION

Multilevel inverters (MLIs) have attracted considerable attention for low-to-high-power conversion applications because of their capacity to reduce harmonics, lower voltage stress, and provide efficient, high-quality output [1], [2]. They have successfully replaced two-and three-level inverters in systems such as static synchronous compensator **(**STATCOM), photovoltaic (PV) power, and electric vehicles [3]–[5]. Conventional MLIs typically include flying capacitor (FC), neutral point clamped (NPC), and cascaded H-bridge (CHB) types. Of these, CHB stands out for its modularity, fault management, and reliability, but it requires multiple isolated DC sources for a staircase output. Conversely, FC and NPC designs require large capacitors, additional passive components, and complex voltage-balancing circuits [6], [7]. Current research focuses on developing MLIs with fewer isolated sources, reduced power semiconductor switches, lower voltage stress, and improved efficiency, and various methods have been proposed to achieve these goals. Recent innovations have involved reconfiguring traditional CHB-MLIs for diverse applications. These MLIs are categorized into switched-dc sources (SS), switched-diodes (SD), and switched-capacitors (SC), employing asymmetrical sources for higher output voltage levels. However, symmetrical MLIs offer simpler control and reduced switching stress. The generalized SS MLIs are detailed in [8] and [9], respectively.

The multilevel inverter in [8] used a rear H-bridge for polarity change, whereas in [9], it is eliminated, significantly reducing the voltage stress. This configuration, as an alternative to CHB-MLI, includes unidirectional switches for both symmetrical and asymmetrical modes. The SD MLI topology presented in [10] is designed for PV usage, whereas the expandable SD MLI in [11] is especially suitable for off-grid PV systems. It reduces the number of switches and drivers and simplifies the control by substituting switches with diodes. These MLIs are particularly efficient for high-resistive loads due to the use of diodes. The CHB-MLI topology in [12] incorporates a self-balanced capacitor-based level-doubling circuit (LDC), nearly doubling the level of voltage while significantly reducing the number of required DC sources. A novel method for reducing DC sources is proposed in [13].

The switched-capacitor multilevel inverter (SCMLI) design minimizes the demand for independent DC sources and multiple power semiconductor switches, while also boosting voltage levels, thereby removing the necessity for large transformers and inductors. This configuration supports both symmetrical and asymmetrical modes of operation. A generalized SCMLI structure [14] generates higher voltage levels through asymmetrical DC source magnitude. The fundamental unit comprises a capacitor, a single DC source, and 2 switches, with one switch charging the SC and the other discharging the SC. The series-parallel charging-discharging method enables capacitor self-regulation at the desired voltage, achieving voltage boosting [15], [16]. Recent SCMLI topologies have focused on boosting factors, load-handling abilities, and voltage stress, with reduced DC source SCMLIs [17]- [19] utilizing a rear H-bridge for polarity changes. However, it require a considerable number of switches, and [19] is unsuitable for high inductive loads. In [20], a non-uniform two-source expandable SCMLI generating a 25-level output voltage waveform with a total standing voltage (TSV) of 20.5 and 13 power semiconductor switches is introduced,

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efficiently reducing power semiconductor switches while attaining a favourable TSV. Inspired by this, the present study introduces a novel twenty-five-level SCMLI module designed to overcome current limitations by minimizing the TSV and system components, with all-capacitor self-balancing without additional voltage balancing equipment.

2. PROPOSED SCMLI TOPOLOGY WORKING

Fig.1 illustrates the circuit schematic for an asymmetrical twenty-five-level SCMLI per phase during the grid-connected operation. This setup generates a 25-level output voltage utilizing twelve power semiconductor switches, two asymmetric DC voltage sources with a quinary ratio two capacitors, and two diodes.

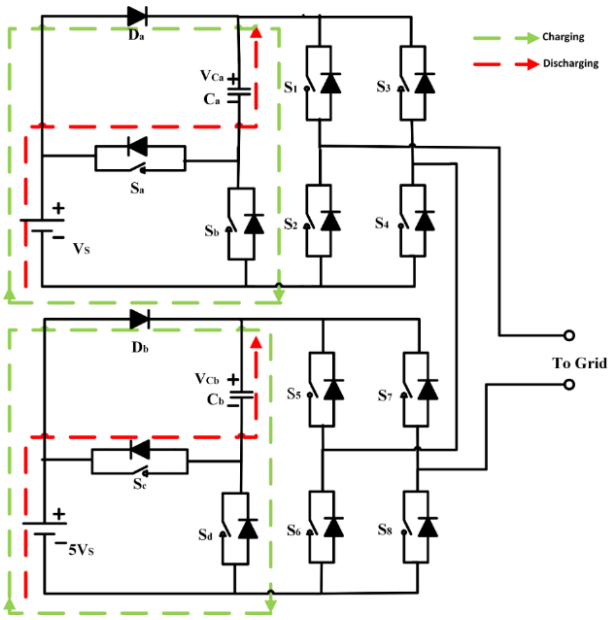


Fig. 1. Per-phase diagram of the proposed 25-level SCMLI.

Table 1 outlines the detailed switching configurations for the proposed SCMLI utilizing a quinary asymmetry ratio, generating a 25-level output. Twenty-five operational modes are identified, each producing distinct output voltage levels.

Utilizing a series-parallel connection technique, switches S_b and S_a can generate voltage levels of V_s and $2V_s$, respectively, whereas switches S_d and S_c can produce voltage levels of $5V_s$ and $10V_s$, respectively. The construction of the two H-bridges involved the utilization of eight switches. The upper H-bridge circuit comprises switches S_1 to S_4, whereas the lower H-bridge circuit comprises switches S_5 to S_8. The power semiconductor switches are controlled in a complementary way using pairs such as (S_1-S_2), (S_3-S_4), (S_a-S_b), (S_5-S_6), (S_7-S_8), and (S_c-S_d). This configuration can produce voltage levels ranging from $0V_s$ to $\pm12V_s$ in steps of V_s, allowing for values such as $\pm V_s$, $\pm2V_s$, $\pm3V_s$, and so on up to $\pm12V_s$. For positive output voltages from the H-bridge circuit S_1 & S_2 and S_5 & S_8 are simultaneously activated, whereas for negative output voltages from the H-bridge circuit S_3 & S_4 and S_6 & S_7 are simultaneously switched-on to achieve the desired output levels of voltage. The proposed MLI inherently balances the capacitor voltage, negating the need for a voltage-balancing control algorithm or sensor circuit.

Table 1. Device modes of the proposed SCMLI.

Switching Modes		Diode Modes	Capacitor Modes	
Main Switches	Charging Switches			
S_1, S_2, S_3, S_4 S_5, S_6, S_7, S_8	S_a, S_b, S_c, S_d	D_a, D_b	C_a, C_b	V_{load} (xV_s)
10011001	1010	00	↓ ↓	12
10011001	0110	10	– ↓	11
01011001	0110	10	– ↓	10
01101001	0110	10	↑ ↓	9
01101001	1010	00	↓ ↓	8
10011001	1001	01	↓ –	7
10011001	0101	11	– –	6
01011001	0101	11	– –	5
01101001	1001	11	↑ –	4
01101001	1001	01	↓ –	3
10010101	0101	01	↓ –	2
10010101	0101	11	– –	1
01010101	0101	11	↑ ↑	0
01100101	1001	11	↑ ↑	-1
01100101	1001	01	↓ –	-2
10010110	1001	01	↓ –	-3
10010110	0101	11	↑ –	-4
01010110	0101	11	– –	-5
01100110	0101	11	– –	-6
01100110	1001	01	↓ –	-7
10010110	1010	00	↓ ↓	-8
10010110	0110	10	↑ ↓	-9
01010110	0110	10	– ↓	-10
01100110	0110	10	– ↓	-11
01100110	1010	00	↓ ↓	-12

3. MODULATION SCHEMES AND CONTROL STRATEGY

This section describes the current control strategy for a 3-phase grid-connected 25-level SCMLI, emphasizing the delivery of both reactive and active power to the grid. Fig. 2 presents a block diagram that illustrates how power is controlled and injected into the grid. The PLL component separates the grid voltage (V_g) into two orthogonal components, V_α and V_β. The current controllers generate a sinusoidal reference depending on the changing demands for reactive power (Q_{ref}) and active power (P_{ref}),

which is then supplied to the level-shifted in-phase disposition (LS-IPD) multicarrier modulation unit. The switching pulses generated by the LS-IPD modulation unit are received by the gate driver circuit of the proposed inverter. Fig. 3 displays the switching signals, while the output voltage generated by the proposed 25-level SCMLI is shown in Fig. 4.

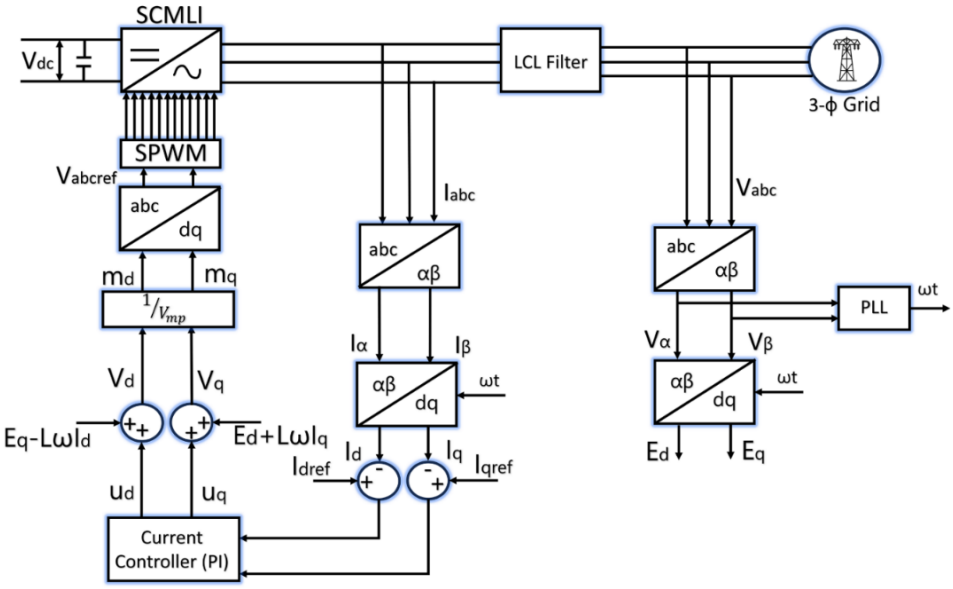


Fig. 2. Grid connected operation of the 25-level SCMLI

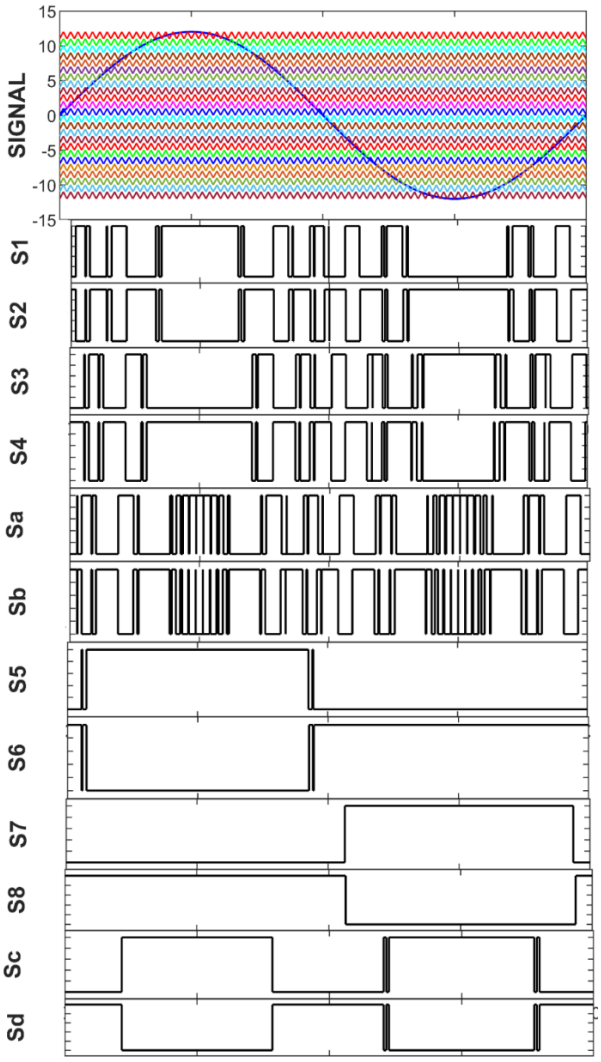


Fig.3. Switching signals derived from LS-IPD multicarrier modulation technique.

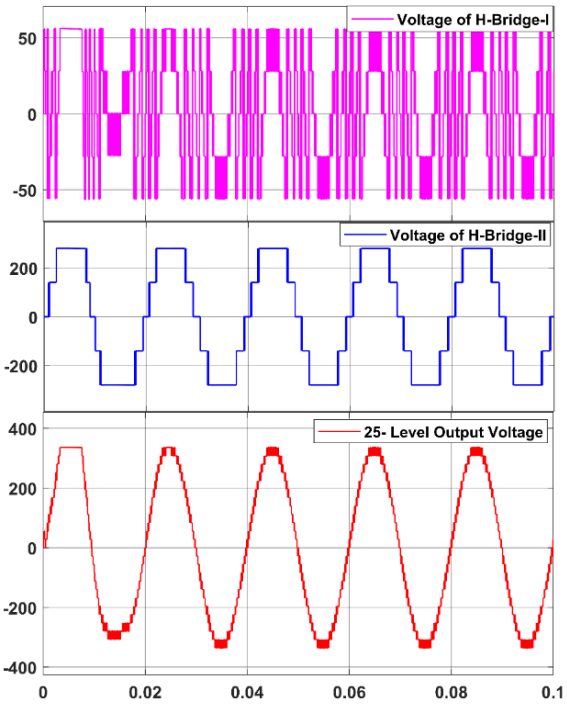


Fig. 4. Output voltage profile of the proposed 25-level per-phase SCMLI.

Table 2. Comparison of the 25-level SCMLIs.

Parameters	[13]	[14]	[15]	[17]	[19]	[20]	Prop. MLI
(N_{sw})	48	36	37	26	16	13	12
(N_{gd})	48	36	37	26	16	12	6
(N_{dc})	6	6	1	2	1	2	2
(N_c)	12	6	11	10	11	2	2
(N_d)	0	6	0	10	22	0	2
(G)	1	2	12	6	2	2	2
TSS (xV_s)	72	60	81	68	60	20.5	10
η%	94.5%	-	-	-	95.5%	96.5%	98.5%

4. COMPARATIVE ANALYSIS

Recent developments in MLI designs utilizing SC techniques allow for both voltage boosting and inherent voltage balancing within the MLI. Additionally, reducing the TSV in MLIs is crucial for optimizing design. This section provides a detailed comparison with recent 25-level SCMLIs, assessing parameters such as the number of switches (N_{sw}), gate drivers (N_{gd}), DC sources (N_{dc}), capacitors (N_c), diodes (N_d), voltage gain (G), total standing voltage (TSV), and inverter efficiency (η%). The tabulated results demonstrate that the proposed 25-level SCMLI not only requires fewer DC voltage sources but also uses fewer system components overall. Furthermore, the complementary switching scheme in the proposed 25-level SCMLI significantly reduces the number of gate drive circuits compared to other configurations. The proposed topology has the lowest TSV of 10 and demonstrates higher efficiency compared to the other topologies, as presented in Table 2.

5. RESULTS AND DISCUSSIONS

This portion presents the efficiency calculation and loss analysis utilizing the piecewise linear electrical circuit simulation (PLECS) software. Furthermore, it analyzes the simulation outcomes obtained using MATLAB software for the injection of 25 kW and 50 kW of active power, along with reactive powers of 25 kVAR and 50 kVAR, under both stable-state and fluctuating power transfer conditions. The parameters utilized in the simulation of the grid-connected 25-level SCMLI are provided in Table 3.

5.1 Calculation of Efficiency for the 25-level SCMLI

PLECS version 4.8.7 is employed to model the 25-level SCMLI and evaluate its efficiency while supplying 25 kW of active power. Both switching and conduction losses are considered when assessing the MLI's efficiency during power delivery to the grid.

Table 3. Specifications of the circuit employed for the grid-integrated functioning of the 25-level SCMLI.

Specifications	Value
Input Voltages	28 V (V_S), 140 V ($5V_S$)
Grid Voltage	415 V
C_1, C_2	4700µF, 4700µF
Switching Frequency $f_{sw,inv}$	3.6 kHz
Output Frequency f_o	50Hz

The conduction loss is caused by the forward voltage drop across the switch when the forward load current passes through the switch, and it can be represented as:

$$P_{conduction_{pd}} = V_{f_{sw}}\, I_{msw} + R_{f_{sw}} I^2_{eff_{sw}} \quad (1)$$

where V_{fsw} and R_{fsw} are the forward voltage drop and forward switch resistance. I_{msw} and I_{effsw} is the mean and effective current flowing through the switch, respectively.

$$P_{sw\_on} = \int_0^{t_{on}} v(t) \times i(t)\, dt \quad (2)$$

By solving (Eqn. 2) P_{sw_on} is expressed as

$$P_{sw\_on} = \frac{V_{ws} I t_{on}}{6} \quad (3)$$

Similarly, P_{sw_off} can be written as

$$P_{sw_{off}} = \frac{V_{ws} I t_{off}}{6} \quad (4)$$

where V_{ws} signifies the switch's withstand voltage, I denote the current passing through the switch, and t_{on} and t_{off} denote the switch's activation and deactivation durations, respectively.

The aggregate switching power dissipation for a complete ON and OFF cycle is determined by:

$$P_{sw,n\_pd} = \left(P_{sw,n\_on} + P_{sw,n\_off}\right) \quad (5)$$

$$P_{sw,n\_pd} = \frac{V_{ws,n} I\left(t_{on} + t_{off}\right)}{6} \quad (6)$$

Efficiency of the inverter is calculated by using the expression as

$$\eta\% = \frac{P_{in} - P_{sw,n_{pd}} - P_{conduction_{pd}}}{P_{in}}\, x\ 100\ \% \quad (7)$$

5.2 Simulation Results

The simulation outcomes for the stable-state operation of the grid-connected 25-level SCMLI are presented, illustrating the injection of active power (50 kW & 25 kW) in Fig.5, reactive power (25 kVA & 50 kVA) in Fig.6, and simultaneous transfer of active power and reactive power (50 kW, 50 kVA and 25 kW, 25kVA) in Fig. 7. The system's performance under different operating conditions is assessed using the control unit. Fig.8 (a) and (b) display the simulated results during load changes from 25 kW to 50 kW and vice versa, while Fig.9 (a) and (b) present the system's response to changes in reactive power from 25kVAR to 50kVAR and vice versa. The grid-connected 25-level SCMLI reaches a stable operating state within a single cycle following changes in the injected grid power. Fig.10 depicts the three-phase grid voltage and current profile in the stable-state condition. The total harmonic distortion (THD) of the output voltage and current waveforms are measured at 4.98% and 3.92%, respectively, while delivering 25 kW of active power to the grid, as shown in Fig. 11.

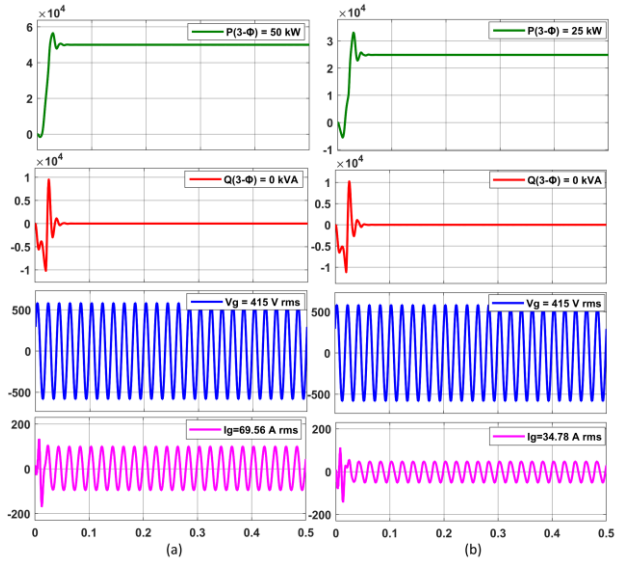


Fig. 5. Simulation outcomes of the grid-connected operation during stable states for (a) 50 kW and (b) 25 kW.

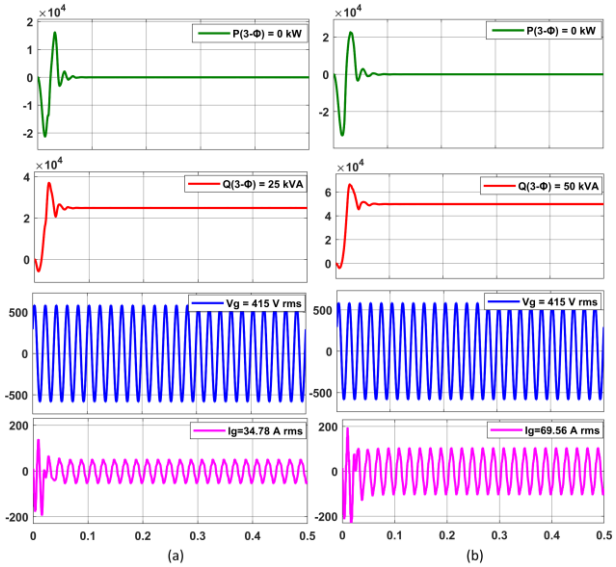


Fig. 6. Simulation outcomes of grid-connected operation during stable states for (a) 25 kVA and (b) 50 kVA.

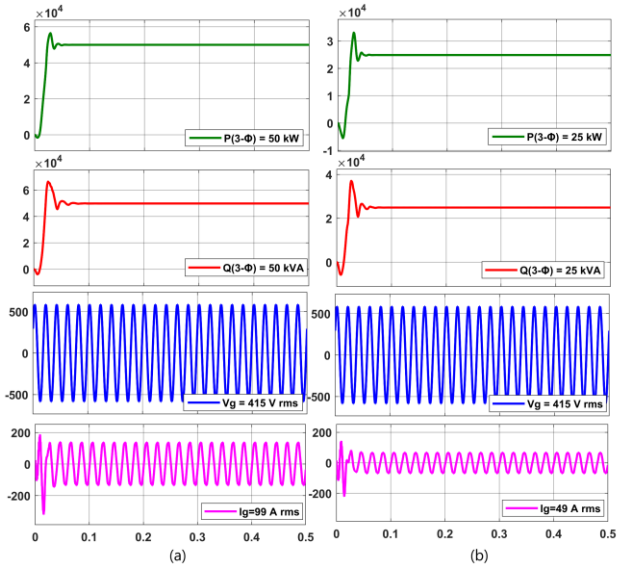


Fig. 7. Simulation outcomes of grid-connected operation during stable state for (a) 50 kW, 50 kVA and (b) 25 kW, 25 KVA.

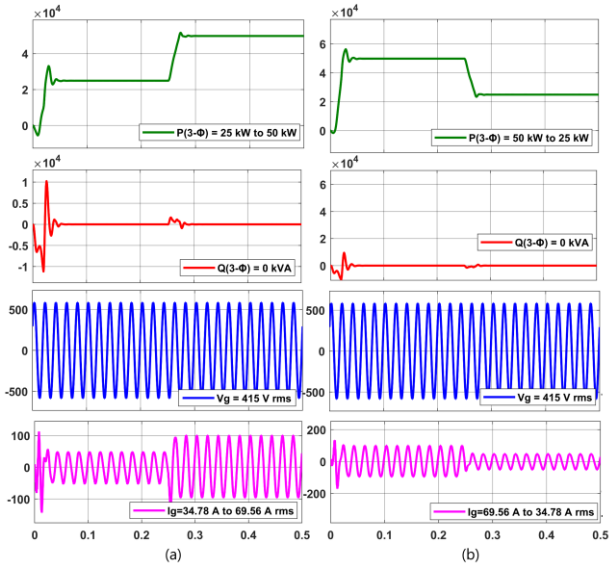


Fig. 8. Simulation outcomes of grid-connected operation for active power transitions from (a) 25 to 50 kW and (b) 50 to 25 kW.

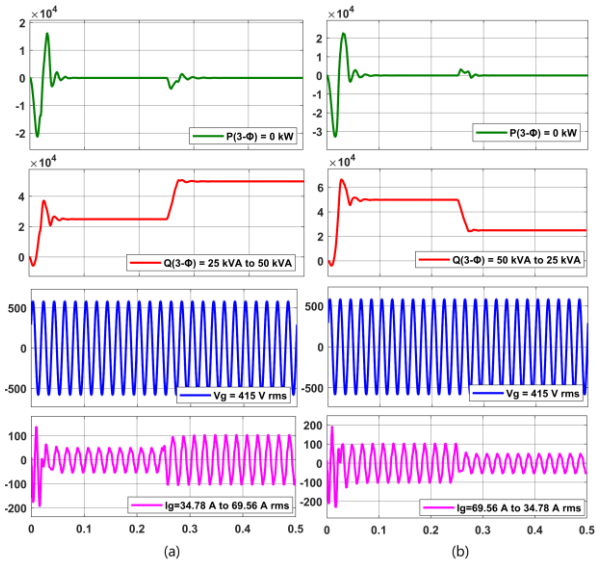


Fig. 9. Simulation outcomes of grid-connected operation for reactive power transitions from (a) 25 to 50 kVA and (b) 50 to 25 kVA.

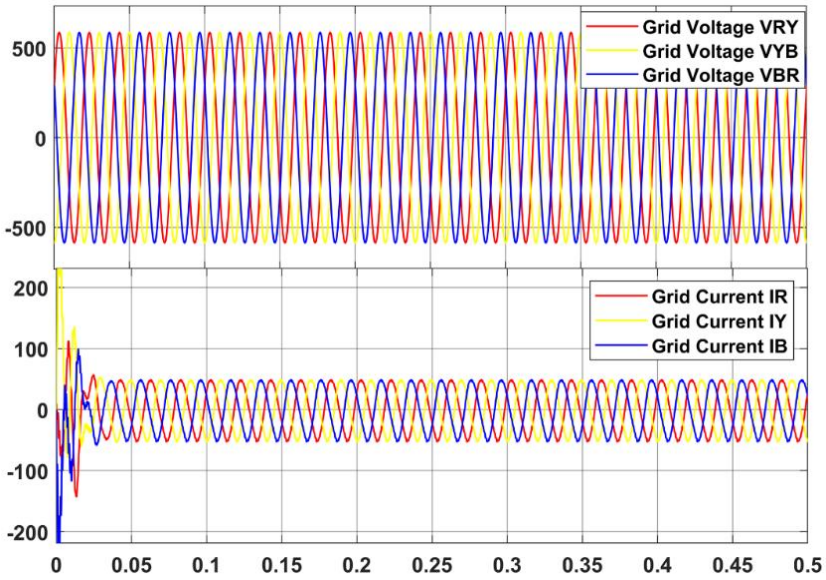
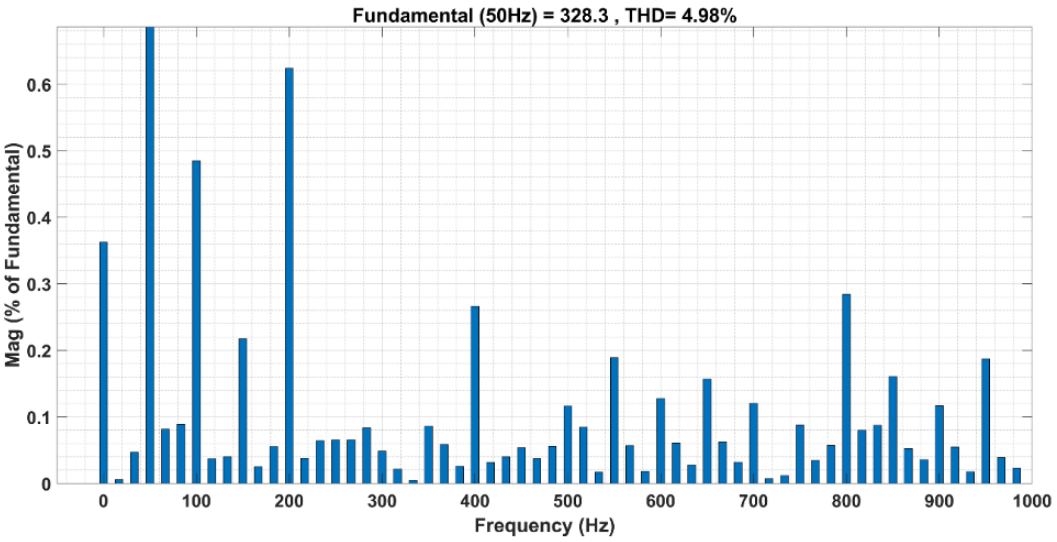
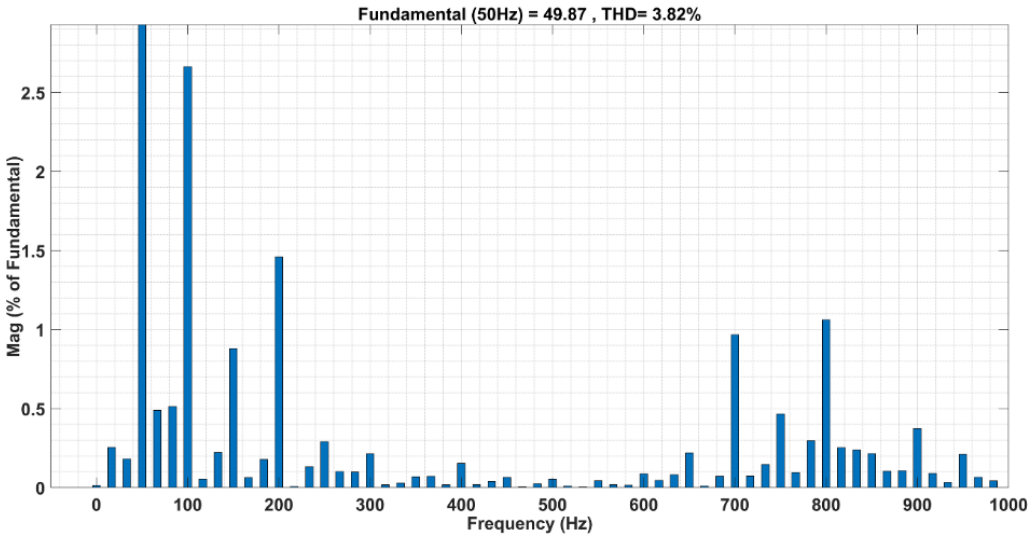


Fig. 10. Three-phase grid voltage and current profile.



(a)



(b)

Fig. 11. THD analysis of (a) output voltage waveform and (b) output current waveform

6. CONCLUSION

This study presented and assessed a novel SCMLI configuration with a quinary asymmetry ratio, utilizing only two DC voltage sources and a reduced component count, capable of producing a 25-level voltage waveform. The SCs are arranged for voltage amplification without additional balancing circuits, which helps in minimizing both the cost and size of the SCMLI. In contrast to conventional MLI designs, this design has a lower switch stress. The gate driver signals are generated using the LS-IPD multicarrier modulation approach. Simulations for grid-connected operations in both stable-state and dynamic scenarios showed compliance with grid requirements, with an inverter voltage and current THD maintained below 5%, in compliance with the IEEE-519 regulations. The inverter efficiency is enhanced to 98.5%, delivering 25 kW of active power to the grid.

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