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Power Flow Control with Static Synchronous Series Compensator (SSSC)

N. Voraphonpiput[*][1], T. Bunyagul[+], and S. Chatratana[#]

Abstract – *The Static Synchronous Series Compensator (SSSC) which is a Series FACT controller, becomes more attractive due to its superior abilities over the impedance-based series compensation. These superior abilities can only be achieved by appropriate control schemes and controller settings. This paper investigates two control schemes of the SSSC for the power flow control. In the first scheme, which is called Reactance Emulation Scheme, the SSSC performs a function of the series impedance connected to the transmission line. This performance can be achieved by controlling the quadrature voltage of the SSSC in relation to the transmission line current, and the required series impedance compensation. In the second control scheme, which is called Quadrature Voltage Control Scheme, the SSSC injects a quadrature voltage into the transmission line. Three modes of compensation, which are capacitive compensation, inductive compensation, and reverse power flow, can be achieved by controlling the phase angle relationship between the injected voltage phasor and line current phasor, and the magnitude of the compensated voltage. A 12- pulse voltage source converter is chosen as the Voltage Source Converter of the SSSC. Dynamic responses of the SSSC with two control schemes are investigated by the digital simulation of a simple two-bus 115 kV 50 Hz power system with a 150 MVA SSSC installed at the sending end bus. Simulation results illustrate good quality of power regulation of the SSSC under both control schemes. Furthermore, the SSSC with quadrature voltage control scheme shows superior performance over the reactance emulation control scheme for its ability to reverse the power flow of the transmission line.*

Keywords – FACTS, Power Flow Control, Quadrature Voltage Control Scheme, Reactance Emulation Scheme, SSSC.

1. INTRODUCTION

The Static Synchronous Series Compensator (SSSC) or (S3C) is a series voltage source based Flexible AC Transmission System (FACTS) controller. The SSSC is usually combined with a Static Synchronous Compensator (STATCOM) and they are operated as a Unified Power Flow Controller (UPFC). However, STATCOM and SSSC can be assigned to operate independently [1]. The SSSC can operate in the Direct Voltage Injection Mode when the STATCOM is not in service. The injected voltage phasor is always kept in quadrature with the transmission line current phasor. Thus, the SSSC provides purely reactive series compensation [2]. The active power flow of the transmission line can be regulated by the control of the magnitude of the SSSC voltage.

This paper describes two control schemes for regulating power flow of the transmission line. In the first scheme, which is called Reactance Emulation Scheme (RES), the SSSC performs as additional series reactors or series capacitors of the transmission line. The power flow of the transmission line decreases when the SSSC operates as series reactors. The power flow increases when the SSSC operates as series capacitors.

In the second scheme, which is called Quadrature Voltage Control Scheme, the SSSC performs as a three-phase AC voltage source and produces voltage phasors, which are in quadrature with the line current phasors. The injected voltage affects the voltage drop across the actual reactance of the transmission line. Consequently, the current flow and power flow of the transmission line can be regulated.

2. PRINCIPLE OF OPERATION OF THE SSSC

The SSSC is generally connected in series with the transmission line with the arrangement as shown in Figure 1. The SSSC comprises a coupling transformer, a magnetic interface, voltage source converters (VSC) and a DC capacitor.

The coupling transformer is connected in series with the transmission line and it injects the quadrature voltage into the transmission line. The magnetic interface is used to provide multi-pulse voltage configuration to eliminate low order harmonics. The VSCs are either two-level converter or three-level converter. One side of the VSC is connected to the magnetic interface while the other side is connected to the DC bus. The VSC generates six-pulse voltage waveform and it is combined into 12 pulse voltage waveform by Wye-Delta connection of the magnetic interface. Higher pulse number (24 or 36 pulses) can be achieved if zigzag transformers are used as the magnetic

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interface. The DC capacitor is used to maintain the DC voltage level of the DC bus. This DC capacitor is selected to meet harmonic and economic criteria of the SSSC and the power system.

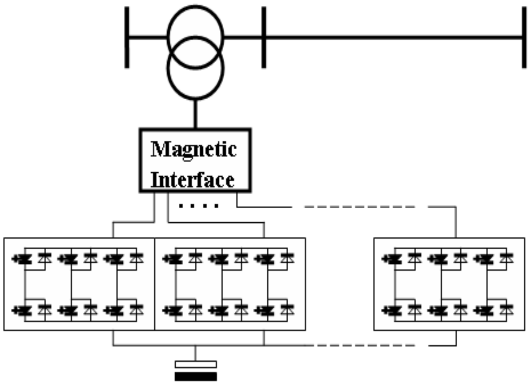

Fig. 1. Diagram of general arrangement of SSSC with the transmission line

The operating principle of the SSSC can be explained using the simple two-bus system with its associated voltage and current phasor diagram in Figure 2.

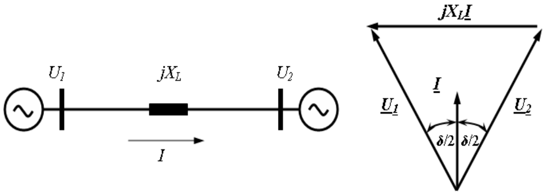

Fig. 2. Simple two-bus power system and its associated phasor diagram

The active power flow between two buses can be expressed as:

$$P_{12} = \frac{U_1 U_2}{X_L} \sin\delta \tag{1}$$

Where, P_{12} is the active power flow from Bus 1 to Bus 2
U_1 is the magnitude of voltage at Bus 1
U_2 is the magnitude of voltage at Bus 2
δ is a phase angle difference between two buses
X_L is the transmission line reactance

The magnitudes of bus voltages are normally regulated within the acceptable range such as ±5% of 1 p.u. The phase angle difference between two buses (δ) is normally low to satisfy the angle stability condition. Therefore, the active power flow mainly depends on the line reactance (X_L).

If the SSSC is series-coupled to the transmission line, it will perform as controlled voltage source. A single line diagram of a transmission line with the series-compensated controllable voltage source and the phasor diagram are presented in Figure 3.

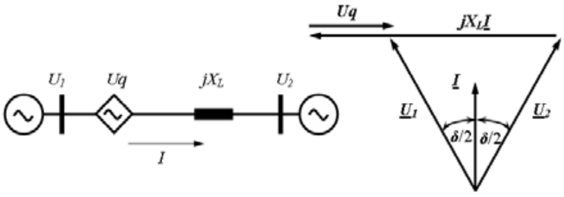

Fig. 3. Two-bus system with the controllable voltage source

The active power flow between two buses (P_{12}) of the compensated transmission line is now expressed as:

$$P_{12} = \frac{U_1 U_2}{X_L} \sin\delta + \frac{U_1 U_q}{X_L} \cos\left(\frac{\delta}{2}\right) \tag{2}$$

Where, Uq is the quadrature voltage injected into the transmission line.

The magnitude of the quadrature voltage (Uq) is directly proportional to the voltage of the DC capacitor in Figure 1. The DC capacitor can be increased or decreased by a small shift of switching angle (firing angle) of the VSC.

It can be observed from Equation 2 that with the same line parameters as in Equation 1 (namely U_1, U_2, δ, and X_L), the active power flow (P_{12}) can be increased or decreased by assigning positive or a negative value to Uq. The relationship between active power and the power angle is shown in Figure 4 for different values of Uq. Note that at a specific δ angle, for example $\delta = 30^o$, the active power flow (P_{12}) for $Uq = 0$ is 0.5 p.u. If $Uq = 0.5$ p.u. is added to the line at this angle, the power can be increased to 1.0 p.u. With $Uq = -1.0$ p.u. the power can even be reversed to –0.5 p.u. It should be noted here that the results, shown in Figure 4, were made on the theoretical basis, to indicate the possibility of control range. Physical rating of components, saturation, and the cost of investment will normally limit the range of the operation in practice.

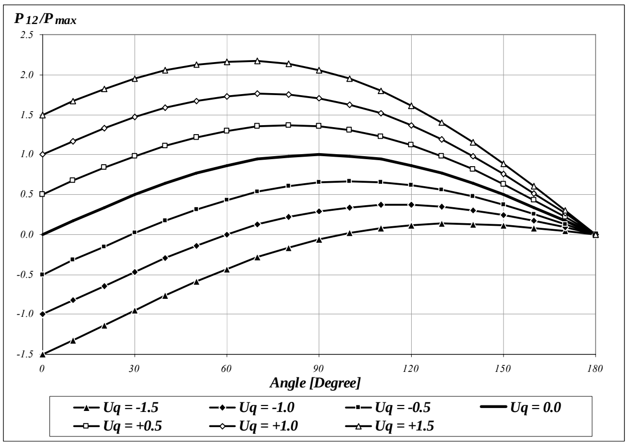

Fig. 4. Power angle curve of the compensated transmission line with controllable series voltage source

3. REACTANCE EMULATION SCHEME

To emulate the function of additional series impedances connected to the transmission line, the quadrature voltage of the SSSC has to be controlled in relation to the transmission line current to achieve the required series impedance compensation.

The controllable series impedance compensator, which is inserted into the transmission line, can be viewed as a means to decrease the reactive line impedance. A single line diagram of a transmission line with series impedance compensation and its phasor diagram are shown in Figure 5.

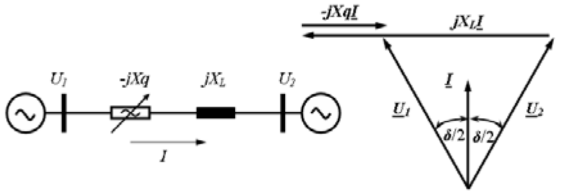

Fig. 5. Two-bus system with series impedance compensation

The total transmission line impedance becomes X_L-X_q and the active power flow can be increased. The active power flow between two buses with series impedance compensation can be expressed as:

$$P_{12} = \frac{U_1 U_2}{X_L(1-k)} \sin\delta \tag{3}$$

Where, Xq is the required series impedance compensation.
k is the compensation ratio of Xq over X_L, $k = \frac{X_q}{X_L}$.

The power equation (Equation 3) can be plotted (in per unit) as a function of δ for various k values as shown in Figure 6. The power angle curves show that power flow of the transmission line increases with the positive compensation ratio (k) and decreases when the compensation ratio (k) is negative.

The ratio of the power flow of the transmission line to P_{max} (k = 0, δ = 90°) can be presented again as a function of the compensation ratio (k) in Figure 7. It can be seen that the active power ratio (P_{12}/ P_{max}) is 1 at k = 0 and decreasing with negative k values (series inductance compensation). On the contrary, the active power flow increases when k is positive and less than 1 (series capacitance compensation).

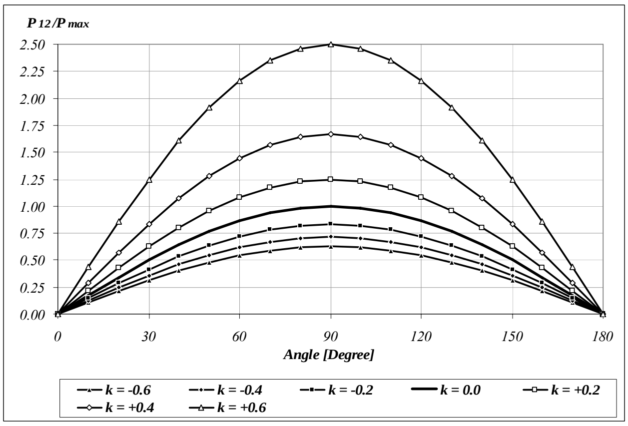

Fig. 6. Power angle curve of the compensated transmission line with the controllable series impedance

The active power flow can also be reversed when the compensation ration k is more than one. In the transmission line point of view, the total reactive line impedance is now capacitive. Moreover, it can also be observed from Figure 7 that the operating point of this system cannot be found when the compensation ratio k equals one because of the resonance between X_L and Xq. In practice, the power flow can be increased up to the thermal limit of the transmission line.

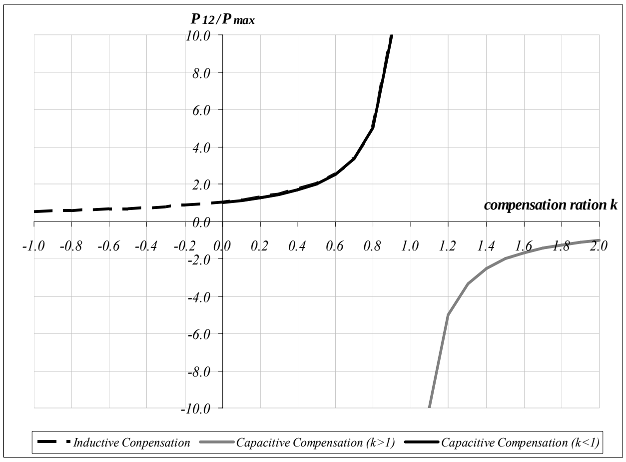

Fig. 7. Relationship between power flow and compensation ratio *k*

From the transmission line standpoint, the controllable series impedance is employed to increase the voltage across the impedance of the given physical line and thereby increasing the line current and the transmitted power. It is important to note that the important parameter is the voltage across the physical line. It follows therefore that the power regulation can also be achieved if the series compensation is provided by a synchronous AC voltage source.

The Reactance Emulation Scheme (RES) is similar to the conventional series compensation. The SSSC acts as a series impedance of the transmission line. Therefore, the injected quadrature voltage (Uq) is a function of the transmission line current (I) and the required series impedance compensation (Xq). The quadrature voltage command (Uq*) can be described as:

$$U_q^* = I X_q^* \tag{4}$$

Where, Uq* is the quadrature voltage command.
I is the transmission line current.
Xq* is the required series impedance compensation.

The block diagram of the Reactance Emulation Scheme (RES), which is modified from [3] and [4], is presented in Figure 8.

The quadrature voltage command can be calculated from the required impedance compensation command (Xq*) and transmission line current (I) as shown in (4). The PI-controller is selected to regulate DC voltage according to the DC voltage command (Udc*), which is calculated from the absolute value of the quadrature voltage command (Uq*). The three-phase line current is measured and fed into the current magnitude calculation block. Result of the magnitude calculation block is fed into the PLL to determine the phase angle of the current (θ_i).

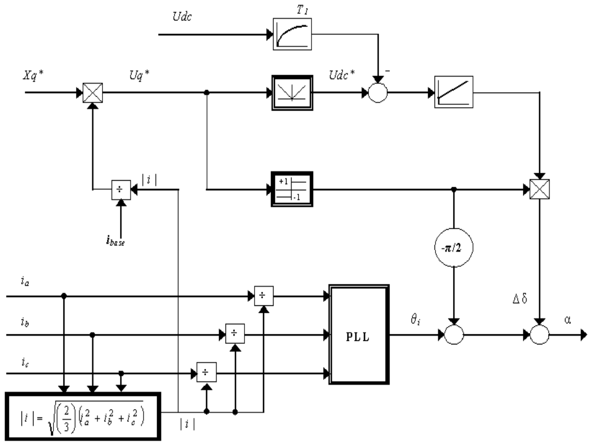

Fig. 8. Block diagram of the Reactance Emulation Scheme (RES)

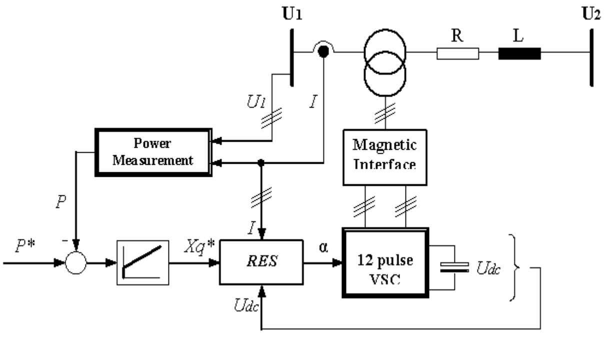

Fig. 9. Block diagram of Power Flow Control with RES

The block diagram of power flow control with RES is shown in Figure 9. It is a cascaded control with the inner loop representing the Reactance Emulation Scheme (RES). The outer loop consists of the power measurement block and a PI-controller. The power flow of the transmission line is measured and compared with the power command (*P**). The result of comparison is fed into the PI-controller, which generates the required impedance compensation command (*Xq**) for the RES block.

4. QUADRATURE VOLTAGE CONTROL SCHEME

The equivalent circuit of a transmission line with SSSC in Figure 10. The voltage sources U_1 and U_2 represent voltages of the sending end and the receiving end, respectively. The series compensated controllable AC source (*Uq*) is the equivalent circuit of SSSC. The transmission line is represented by a series connection of an equivalent resistor (*R*) and inductor (*L*). The transmission line current is defined to flow from Bus 1 to Bus 2. Phasor diagram of the transmission line with SSSC in three operation modes are shown in Figure 11.

It should be noted that all phasor diagrams in Figure 11 were not drawn to scale. They were exaggerated to show the effect of compensation on the current flow. In normal operation, the voltage phasor $\underline{U}_1$ leads the voltage phasor $\underline{U}_2$ with δ degrees. The voltage across the transmission line is represented by phasor $\underline{U}_T$, which consists of the voltage across the inductor $\underline{U}_{XL}$ and the voltage across the resistor $\underline{U}_R$. The phasor $\underline{I}$ represents transmission line current.

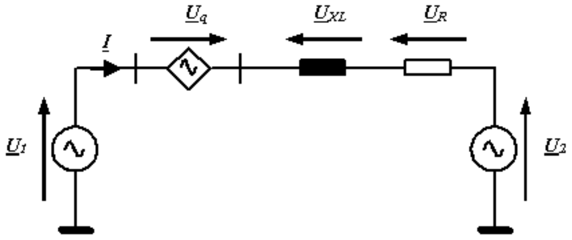

Fig. 10. Equivalent circuit of SSSC system

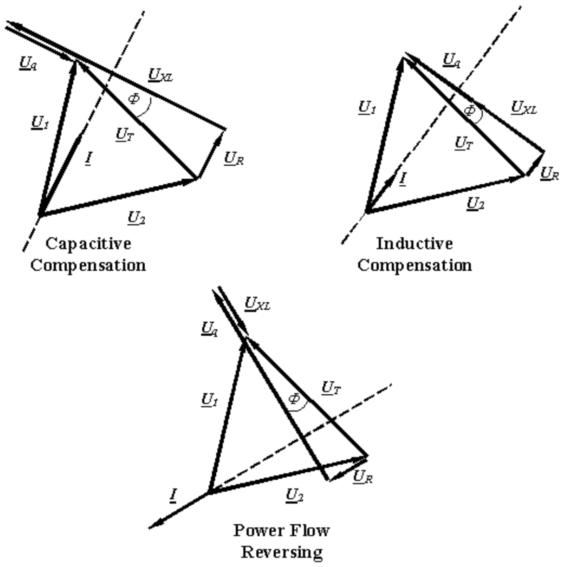

Fig. 11. Phasor diagram of three operation modes (a) capacitive compensation (b) inductive compensation, and (c) power flow reversing

The capacitive compensation by SSSC is shown in Figure 11(a). The quadrature voltage phasor $\underline{Uq}$ is in the opposite direction of the $\underline{U}_{XL}$ and $\underline{Uq}$ lags the current phasor $\underline{I}$ by 90°. For the same total voltage drop $\underline{U}_T$, the voltage phasor across line reactance ($\underline{U}_{XL}$) increases and results in the increase of power flow.

The inductive compensation is shown by the phasor diagram in Figure 11(b). The quadrature voltage is in the same direction of the $\underline{U}_{XL}$ and $\underline{Uq}$ leads the current phasor $\underline{I}$ by 90°. For constant $\underline{U}_T$, $\underline{U}_{XL}$ decreases. The transmission line current reduces and results in the reduction of the power flow.

The ability of SSSC to reverse power flow is demonstrated by the phasor diagram in Figure 11(c). The operation is similar to the inductive compensation but the VSC voltage will be further increased until it is larger than the magnitude of $\underline{U}_{XL}$. For constant $\underline{U}_T$, $\underline{U}_{XL}$ and $\underline{U}_R$ reverse their directions. The current phasor $\underline{I}$ and hence power flow reverse.

The Quadrature Voltage Control Scheme (QVCS), which is modified from [5], is shown in Figure 12. This scheme offers three operating modes with stable operation during power reversal. The QVCS consists of a measurement system, controller, and logical switch block. The main function of the control loop is to maintain DC voltage according to the quadrature voltage command (*Uq**). The DC voltage (*Udc*) is measured and compared with the DC voltage command (*Udc**), which is calculated from an absolute value of the quadrature voltage command (|*Uq**|). The result of comparison is fed into a proportional plus integral controller (PI-controller). The PI-controller is used to control the DC voltage by generating appropriate phase angle signal ($\Delta\delta$). Parameters of the PI-controller, which are the proportional gain (Kp) and the integrator time constant (Tn), are tuned to achieve fast dynamic response of the inner control loop.

There are two logical switches which assign an appropriate switching angle of the SSSC according to each operating mode. The logical switches are controlled by signal from the quadrature voltage command (Uq^*). The magnitude and polarity of the quadrature voltage command (Uq^*) is determined in the upper part of the diagram in Figure 12.

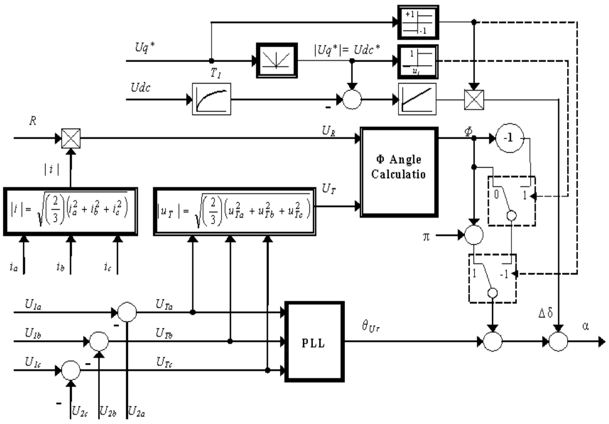

Fig. 12. Block diagram of Quadrature Voltage Control Scheme

The three-phase bus voltage of Bus 1 and Bus 2 are measured and used for the calculation of the voltage drop of the transmission line (U_T). The Phase Locked Loop (PLL) uses these signals to calculate phase angle (θ_{UT}). The magnitude $|u_T|$ is also calculated from the three-phase U_T signals (U_{Ta}, U_{Tb}, U_{Tc}). The three phase line currents are measured and used for the calculation of resistive voltage drop (U_R). The signals $|u_T|$ and U_R are used to calculate the angle Φ.

The conditions of command Uq^* and firing angle for three operating modes are given below:

1. Capacitive compensation: $Uq^* > 0$
   $$\alpha = \Delta\delta + \theta_{UT} + \Phi + \pi$$
2. Inductive compensation: $Uq^*<0$ an $|Uq^*|<U_T$
   $$\alpha = \Delta\delta + \theta_{UT} + \Phi$$
3. Reversing power flow: $Uq^*<0$ and $|Uq^*|>U_T$
   $$\alpha = \Delta\delta + \theta_{UT} - \Phi$$

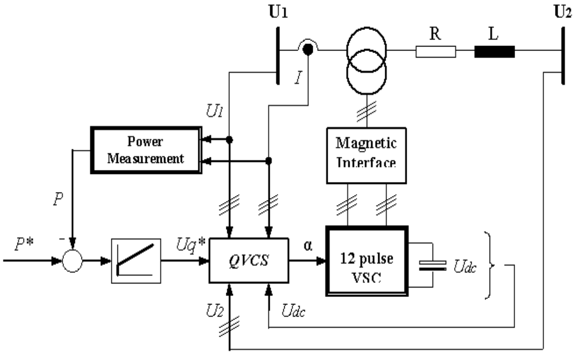

Fig. 13. Block diagram of Power Flow Control with QVCS

The block diagram of the cascaded power flow control is shown in Figure 13. The quadrature voltage control scheme (QVCS), forms an inner loop of Figure 13. The power flow is calculated from voltage and current at Bus 1 by a power measurement block. Only one PI-controller is used in the outer loop to control the power flow of the transmission line. This controller generates the appropriate quadrature voltage command (Uq^*) for the quadrature voltage control block.

5. SIMULATION RESULTS

The two-bus 115 kV 50 Hz system with SSSC as shown in Figure 14 was simulated with PSCAD/EMTDC. The transmission line parameters are L = 36.4 mH and R = 0.3997 Ω. The system base MVA is 200 MVA and the rating of SSSC is 150 MVA. The rating of the coupling transformer is 150 MVA and 20kV/20kV voltage winding. The magnetic interface comprises two banking transformers which the primary windings are connected in series with the coupling transformer while the secondary windings are connected in Wye and Delta, respectively. The Wye and Delta connection are connected to a two-level voltage source converter. The rating of both transformers, which act as the magnetic interface, are 25 MVA and voltage windings are 10 kV/5.77 kV and 10 kV/10 kV respectively. Each transformer is modeled with 5% impedance. A 1,500 μF capacitor is chosen for DC bus capacitor. Phase voltage at sending end bus leads the receiving end bus by 10 degrees. The SSSC base voltage is 16.365 kV (peak). The system base phase voltage is 93.9 kV (peak). The transmission line base current is 1.429 kA. The base DC voltage is 9.09 kV.

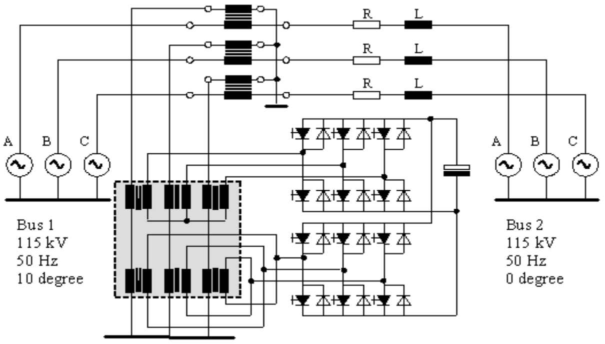

Fig. 14. The circuit diagram of two bus 115 kV 50 Hz system with SSSC

Reactance Emulation Scheme (RES)

The simulation results of the power flow control with Reactance Emulation Scheme (RES) in Figure 9 are shown in Figures 15 to 20. The system and SSSC under the RES was tested with six events as shown by the power command (P^*) changes in Figure 15. Power flow of the transmission line was first regulated at 1.5 p.u.. The power flow command (P^*) was changed in the first event from 1.5 p.u. to 1.25 p.u. at t =1.0 sec. Power flow of the transmission line decreased to 1.25 within 0.1 sec. and it took 0.2 sec. to settle. The power flow command (P^*) was changed back to 1.5 p.u. in the second event at 1.5 sec. The third event was the same as the first one. In the fourth event at 2.5 sec., the power flow command (P^*) was reduced from 1.25 p.u. to 0.75 p.u. Power flow response reduced to 0.75 p.u. within 0.1 sec. and it also took 0.2 sec. to settle. The fifth event occurred at t = 3.0 sec, when power flow of the transmission line was reduced further from 0.75 p.u. to 0.5 p.u. It could be observed that there is no overshoot of the power flow in this event. Moreover, it could be seen from Figure 15 that the dynamic response of each event was not similar. This is because of the nonlinearity due to the multiplication of required impedance compensation and transmission line current. The power reversing mode could not be performed with this control scheme.

Active power (P_{SSSC}) and reactive power (Q_{SSSC}) of the SSSC during all operations with RES are shown in Figure 16. The SSSC generated reactive power during the first event to the third event. It absorbed reactive power at the fourth event to the sixth event. It could be seen that the active power consumed by SSSC was very small.

The DC capacitor voltage is shown in Figure 17. It varied according to the power flow command (P^*). It can be observed that the ripples of DC voltage during increasing power flow operation (the first event to the third event) are higher than during decreasing power flow operation (the fourth event to the sixth event).

The voltage waveform of the sending end bus (U_1), the transmission line current waveform (I) and the injected quadrature voltage waveform (Uq) of the first event up to the fourth event, except the third event, are presented in Figures 18 to 20.

Fig. 15. Active power and reactive power flow of the transmission line (RES)

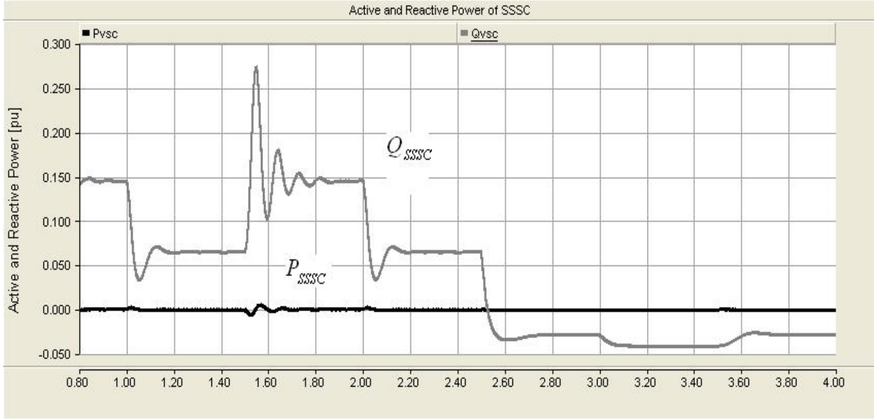

Fig. 16. Active power and reactive power flow of SSSC

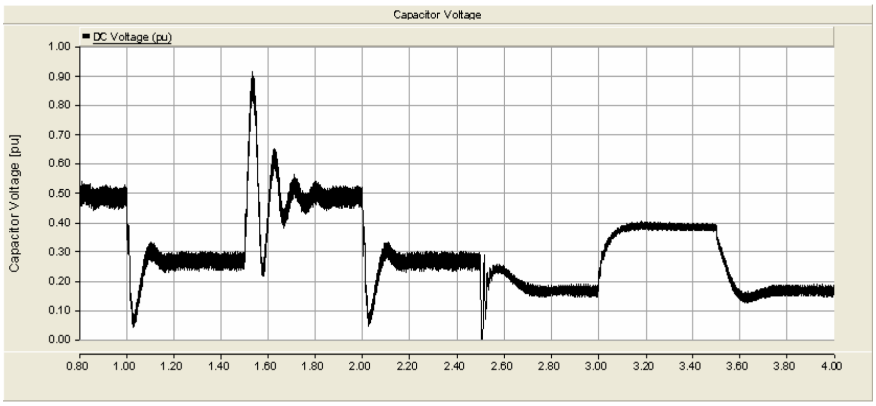

Fig. 17. DC capacitor voltage

Figure 18 shows the injected quadrature voltage (*Uq*) and line current (*I*) waveforms during the first event (t = 1.0 sec). The injected quadrature voltage (*Uq*) was not a perfectly sinusoidal waveform because the 12-pulse voltage source converter was applied in this case. In the first event, the active power command (*P**) reduced from 1.5 p.u. to 1.25 pu. Therefore, the injected quadrature voltage (*Uq*) reduced its magnitude according to the required impedance compensation command (*Xq**), which resulted in decreasing of the line current (*I*). The SSSC performed capacitive compensation mode which can be confirmed by the waveform of the injected voltage which lagged the line current by almost 90 degrees.

Figure 19 shows the injected quadrature voltage (*Uq*) and line current (*I*) waveforms during the second event (t = 1.5 sec), when the active power command (*P**) was increased from 1.25 p.u. to 1.5 pu. It could be observed than the injected quadrature voltage (*Uq*) and the line current (*I*) had high fluctuation due to nonlinear characteristic of the reactance compensation. The SSSC operated in the capacitive compensation mode.

Figure 20 presents injected quadrature voltage (*Uq*) and line current (*I*) waveform during the fourth event (t = 2.5 sec). The SSSC changed the mode of operation from capacitive compensation to inductive compensation. The phase angle of the injected quadrature voltage (*Uq*) reversed from 90 degrees lagging to 90 degrees leading with respect to the line current (*I*) and the reversal process took 2 cycles to complete. The line current (*I*) and the active power flow (*P*) of the transmission line were reduced.

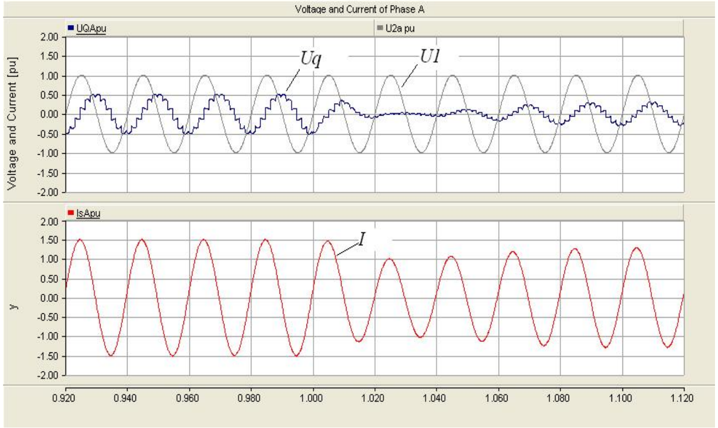

Fig. 18. Voltage (U_1), current (*I*) and quadrature voltage (*Uq*) during the first event (phase A)

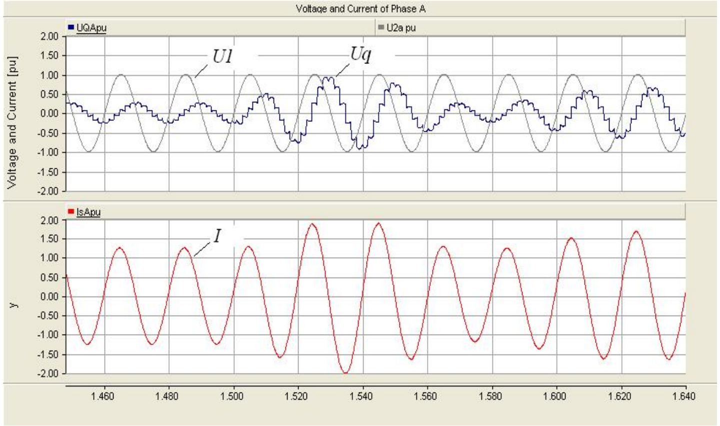

Fig. 19. Voltage (U_1), current (*I*) and quadrature voltage (*Uq*) during the second event (phase A)

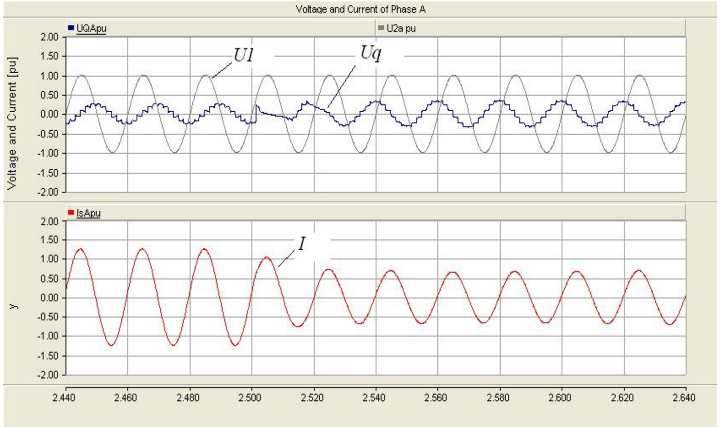

Fig. 20. Voltage (U_1), current (*I*) and quadrature voltage (*Uq*) during the fourth event (phase A)

It should be noted that control characteristic of the SSSC under Reactance Emulation Scheme (RES) behaves like a low damped system when operates in the capacitive compensation mode and behaves like a high damped system when operates in the inductive compensation mode. This nonlinear characteristic of the RES must be taken into account in the design of the control system.

Quadrature Voltage Control Scheme (QVCS)

The power flow control with QVCS in Figure 13 was applied to the system in Figure 15 and simulated on PSCAD/EMTDC. The control system with QVCS was tested with five events as shown by the power command signal (*P**) in Figure 21. The system started with the power flow command *P** of 1.25 p.u. The first event occurred at 1.5 sec, when the power flow command (*P**) was increased from 1.25 p.u. to 1.5 p.u. The power flow of the line increased to the new value within 0.1 sec and settled at t = 1.8 sec. The second event occurred at 2.0 sec., when the power flow command (*P**) was switched back to 1.25 p.u. The SSSC performed as a capacitive compensation during the first and the second events.

The third event occurred at 2.5 sec., when the power flow command (*P**) was reduced further to 0.5 p.u. and the mode of operation of the SSSC changed from capacitive to inductive compensation. The power flow took 0.2 sec. to settle to the new value of 0.5 p.u.

The fourth event and the fifth event were power reversing mode. It could be seen that the power flow of the line reduced to -0.5 p.u. at t = 3.0 sec. and then returned to 0.5 p.u. at t = 3.5 sec. It can be observed that the reactive power flow (*Q*) of the transmission line changed very little during the whole operation.

The active power (P_{SSSC}) and the reactive power (Q_{SSSC}) response of the SSSC during all events are shown in Figure 22. The SSSC generated reactive power (capacitive compensation) during the first event and the second event. It absorbed reactive power (inductive compensation) during the third event and generated the reactive power again when it performed in power reversing mode. It could also be seen that the active power of the SSSC was very small because the SSSC consumed active power only to maintain internal losses of the converters and the transformers.

The DC capacitor voltage responses are shown in Figure 23. It varied due to the quadrature voltage command (*Uq**). It could be observed that the DC capacitor voltage was higher than 1.0 p.u. during 3.0 sec. to 3.5 sec. because the SSSC operated in the power reversing mode during this period of time.

Fig. 21. Active power and reactive power flow of the transmission line (QVCS)

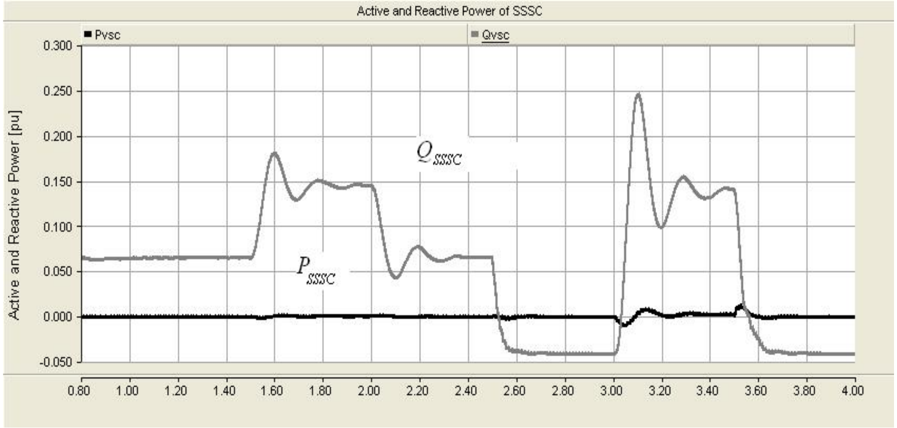

Fig. 22. Active power and reactive power flow of SSSC

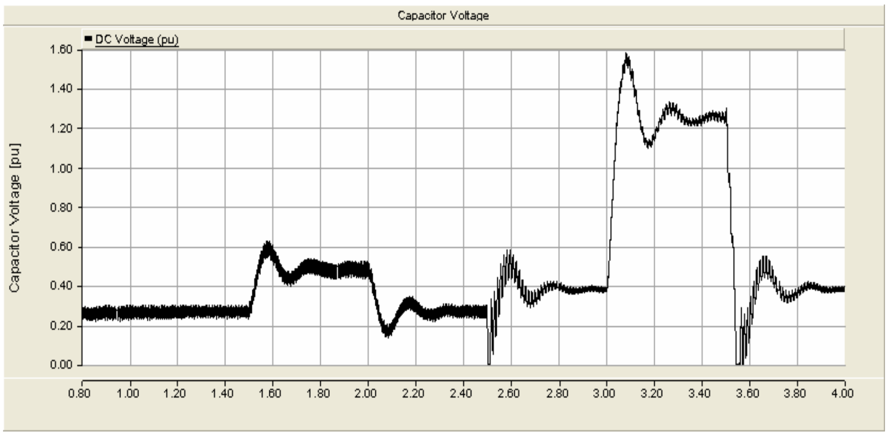

Fig. 23. DC capacitor voltage

The voltage waveform of the sending end bus (U_1), the transmission line current waveform (I) and the injected quadrature voltage waveform (Uq) during five events were presented in Figures 24 to 28.

Figure 24 presents the injected quadrature voltage waveform (Uq) and line current (I) waveforms during the first event (t = 1.5 sec) where the power command (P^*) was increased from 1.25 p.u. to 1.5 p.u.. The injected quadrature voltage (Uq) increased its magnitude and resulted in increasing of the line current. The SSSC performed capacitive compensation in this event because the injected quadrature voltage (Uq) lagged the line current (I) by almost 90 degrees.

In Figure 25, the injected quadrature voltage waveform (Uq) and line current (I) waveforms during the second event (t= 2.0 sec) are presented. The power command (P^*) was reduced from 1.5 p.u. to 1.25 p.u.. The injected quadrature voltage (Uq) reduced its magnitude and resulted in the reduction of line current.

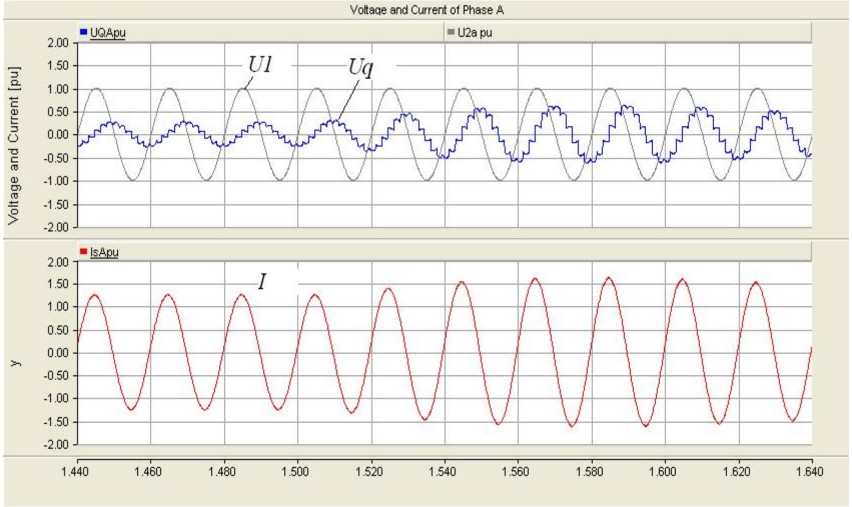

Fig. 24. Voltage (U_1), current (I) and quadrature voltage (Uq) during the first event (phase A)

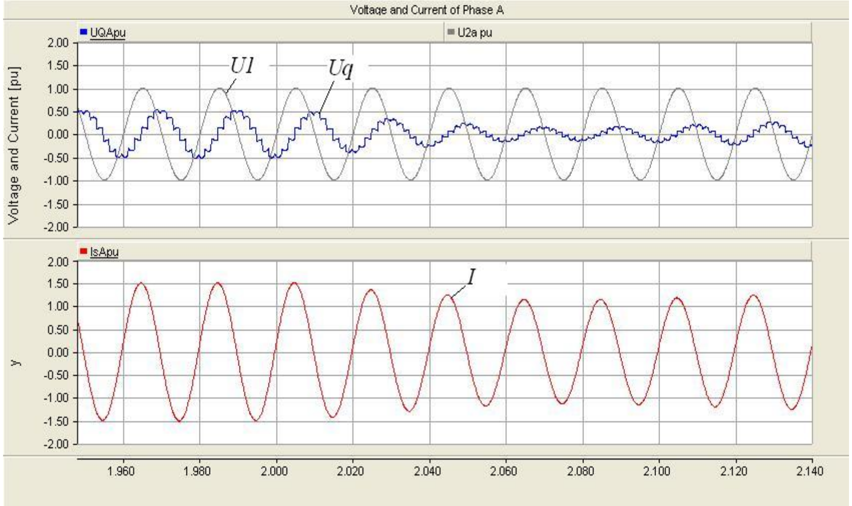

Fig. 25. Voltage (U_1), current (I) and quadrature voltage (Uq) during the second event (phase A)

Figure 26 presents the injected quadrature voltage waveform (*Uq*) and line current (*I*) waveforms during the third event (t = 2.5 sec). The power command (*P**) was reduced from 1.25 p.u. to 0.5 p.u. Thus, mode of operation of the SSSC was changed from capacitive compensation to inductive compensation, which could be seen from the reversing of the phase angle of the injected quadrature voltage (*Uq*). The phase reversing process took approximately 1 cycle to complete.

Figure 27 presents the injected quadrature voltage waveform (*Uq*) and line current (*I*) waveforms during the fourth event (t = 3.0 sec). The power command (P*) was reversed from +0.5 p.u. to -0.5 p.u.. The magnitude of injected quadrature voltage (*Uq*) increased to be more than 1.0 p.u. which means that the injected quadrature voltage (*Uq*) is higher than the voltage drop across the transmission line (U_T). When the magnitude of the injected quadrature voltage was close to voltage drop across the transmission line, the line current was close to zero (t = 3.02 sec). After that, the injected quadrature voltage (*Uq*) was higher and the phase angle of the line current (*I*) reversed. The SSSC operated in the power reversing mode. It can be observed that phase angle difference of the line current and the sending end voltage (U_1) is almost 180 degrees during the power reversing mode.

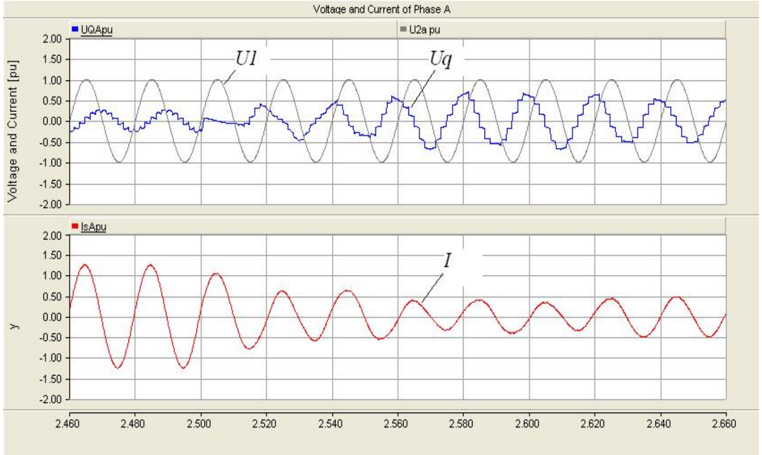

Fig. 26. Voltage (U_1), current (*I*) and quadrature voltage (*Uq*) during the third event (phase A)

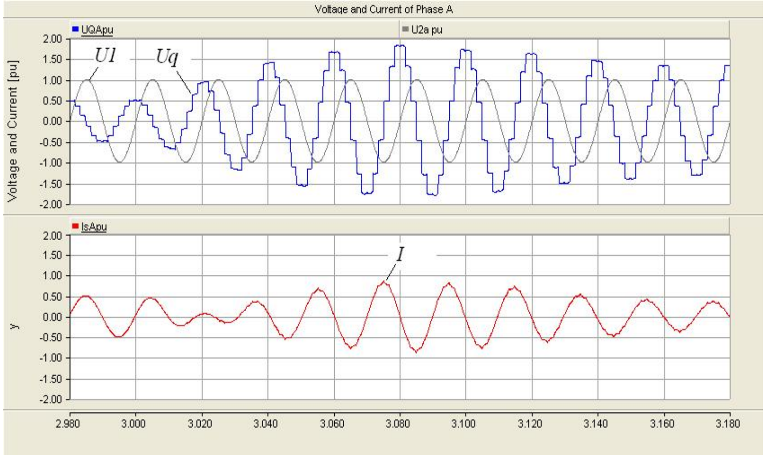

Fig. 27. Voltage (U_1), current (*I*) and quadrature voltage (*Uq*) during the fourth event (phase A)

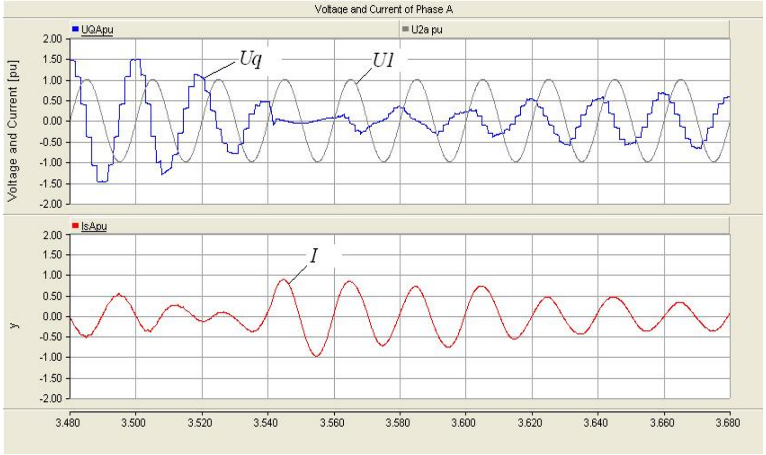

Fig. 28. Voltage (U_1), current (*I*) and quadrature voltage (*Uq*) during the fifth event (phase A)

Figure 28 presents the injected quadrature voltage waveform (*Uq*) and line current (*I*) waveforms during the fifth event (t = 3.5 sec). The power command (*P**) was reversed back from -0.5 p.u. to +0.5 p.u.. The injected quadrature voltage (*Uq*) reduced to be less than 1.0 p.u. and the phase angle of the line current (*I*) reversed back and the injected quadrature voltage (*Uq*) lead the line current (*I*) by almost 90 degrees.

Dynamic behaviors of the SSSC under Quadrature Voltage Control Scheme (QVCS) did not differ very much. Namely, system damping of the SSSC during three operating modes did not change significantly. It is noted here that the characteristic of SSSC with QVCS is more linear when compared with the SSSC with RES. This is because the RES is based on impedance compensation which has nonlinearity power angle curve as shown in Figure 6 whereas the QVCS is based on inserted controllable voltage source, which has linearity power angle curve as shown in Figure 4. An ability of the SSSC to reverse power flow direction as shown in Figure 4 was illustrated by the simulation of the control system with Quadrature Voltage Control Scheme.

6. CONCLUSION

This paper presented two schemes of power flow control of SSSC which are the Reactive Emulation Scheme (RES) and the Quadrature Voltage Control Scheme (QVCS). Theoretical analysis and simulation results computer simulations show that the SSSC can effectively regulate the active power flow of the transmission line. Active power could be increased and decreased effectively with the SSSC under the QVCS and the RES. However, the SSSC with the QVCS showed the superior performance over the RES in its ability to reverse the flow of the transmission line and the linearity of the system characteristic.

The dynamic responses of the voltage and current waveform were fast. It took 1 cycle in average to change the magnitude or to reverse the phase angle. It can be concluded that the SSSC with the two control schemes offer good performance for the power flow regulation. It should be noted that, many practical considerations in terms of component rating, saturation, range of operation, and harmonic contents have to be taken into account in the design and construction of the SSSC.

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